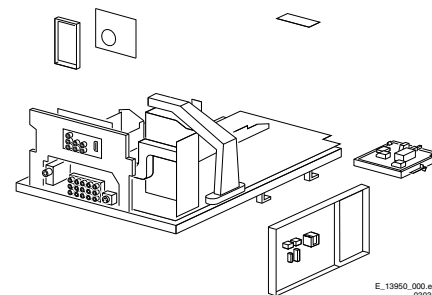


# Service Service Service

# A02U AA



# Service Manual

## Contents

	Page	
1. Technical Specifications, Connections, and Chassis Overview	2	
2. Safety Instructions, Warnings, and Notes	4	
3. Directions for Use	6	
4. Mechanical Instructions	8	
5. Service Modes, Error Codes, and Faultfinding	11	
6. <i>Block Diagrams, Testpoint Overviews, and Waveforms</i>		
Wiring Diagram	21	
Block Diagram LSP Supply and Deflection	22	
Testpoint Overview LSP and CRT	23	
Block Diagram 1 Audio & Video	24	
Block Diagram 2 Audio & Video	25	
Testpoint Overview SSB	26	
I2C Overview	27	
Supply Lines Overview	28	
7. <i>Circuit Diagrams and PWB Layouts</i>		<i>Diagram PWB</i>
LSP: Main Supply (Diagr. A1A)	29	39-44
LSP: Main Supply (Diagr. A1B)	30	39-44
LSP: Standby Supply (Diagr. A2)	31	39-44
LSP: Line Deflection (Diagr. A3)	32	39-44
LSP: Frame Defl. & E/W Drive (Diagr. A4)	33	39-44
LSP: Rotation Circuitry (Diagr. A5)	34	39-44
LSP: Headphone Amplifier (Diagr. A7)	34	39-44
LSP: Audio Amplifier (Diagr. A6)	35	39-44
LSP: Tuner SIMM Conn. (Fem.) (Diagr. A8)	36	39-44
LSP: Front (Diagr. A10)	37	39-44
LSP: Inputs/Outputs (Diagr. A11)	38	39-44
SSB: If & SAW Filter (Diagr. B1)	45	62-63
SSB: Video Source Sel. & Data Link (Diagr. B2)	46	62-63
SSB: Audio Source Select (Diagr. B3)	47	62-63
SSB: MPIF-Supply, E.W., & Control (Diagr. B4)	48	62-63
SSB: Video Decoder (Diagr. B5)	49	62-63
SSB: Feature Box (Diagr. B6)	50	62-63

## Contents

	Page	
SSB: RGB Processing (Diagr. B7)	51	62-63
SSB: Sync & Deflection Proc. (Diagr. B8)	52	62-63
SSB: Protection (Diagr. B9)	53	62-63
SSB: Audio Processing (Diagr. B10)	54	62-63
SSB: Control (Diagr. B11)	55	62-63
SSB: Contr.-Mem.y Interf. (EBIU) (Diagr. B12)	56	62-63
SSB: Contr.-Mem. Interf. (SDRAM) (Diagr. B13)	57	62-63
SSB: ADOC Supply (Diagr. B14)	58	62-63
SSB: Low Voltage Supply ADOC (Diagr. B15)	59	62-63
SSB: 3D COMB Filter (Diagr. B17)	60	62-63
SSB: Connector Interface (Diagr. B18)	61	62-63
Side I/O Panel (Diagr. D)	64	65
CRT Amplifier (Diagr. F1)	66	68-69
Auto SCAVEM (Diagr. F2)	67	68-69
DC Shift Panel (Diagr. G)	70	70
VDAF Panel + 2nd Orders (Diagr. I)	71	72
Front Interface Panel (FL13) (Diagr. J)	73	74
Front Interface Panel (PV2) (Diagr. J)	75	76
HDMI: Panellink Receiver (Diagr. M1)	77	80-81
HDMI: Input Selection (Diagr. M2)	78	80-81
HDMI: Sync Selection & I/O Exp. (Diagr. M3)	79	80-81
Side I/O Panel (Diagr. O)	82	83
Top Control Panel (FL13) (Diagr. P)	84	85
Top Control Panel (PV2) (Diagr. P)	86	87
8. Alignments	89	
9. Circuit Descriptions	98	
Abbreviation List	112	
IC Data Sheets	115	
10. Spare Parts List (not applicable)	117	
11. Revision List	118	

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# PHILIPS

# 1. Technical Specifications, Connections, and Chassis Overview

Index of this chapter:

1. Technical Specifications
2. Connections
3. Chassis Overview

**Note:** Figures below can deviate slightly from the actual situation, due to the different set executions.

## 1.1 Technical Specifications

### 1.1.1 Vision

Display type	: DV-CRT-RF
Screen size(s)	: 26 inch - 16:9
	: 27 inch - 4:3
	: 30 inch - 16:9
	: 32 inch - 4:3
	: 34 inch - 16:9
Tuning system	: PLL
IF frequency	: 45.75 MHz
Color systems	: NTSC M (3.58-4.5)
Channel selections	: 181 presets
	: Full cable, UHF
Video playback	: ATSC
	: 480p
	: 1080i
Aerial input	: 75 ohm, F-type

### 1.1.2 Sound

Sound systems	: BTSC DBX
Maximum power	: 2 x 10 W <sub>rms</sub> (int.)

### 1.1.3 Miscellaneous

Mains voltage	: 110 V <sub>ac</sub>
Mains frequency	: 50 / 60 Hz
Ambient temperature	: +5 to +45 deg. C
Maximum humidity	: 90 % R.H.

Power consumption	
- Normal operation	: ≈ 159 W
- Standby	: < 1 W

## 1.2 Connections

**Note:** The following connector color abbreviations are used (acc. to DIN/IEC 757): Bk= Black, Bu= Blue, Gn= Green, Gy= Grey, Rd= Red, Wh= White, Ye= Yellow.

### 1.2.1 Top Control and Front / Side Connections

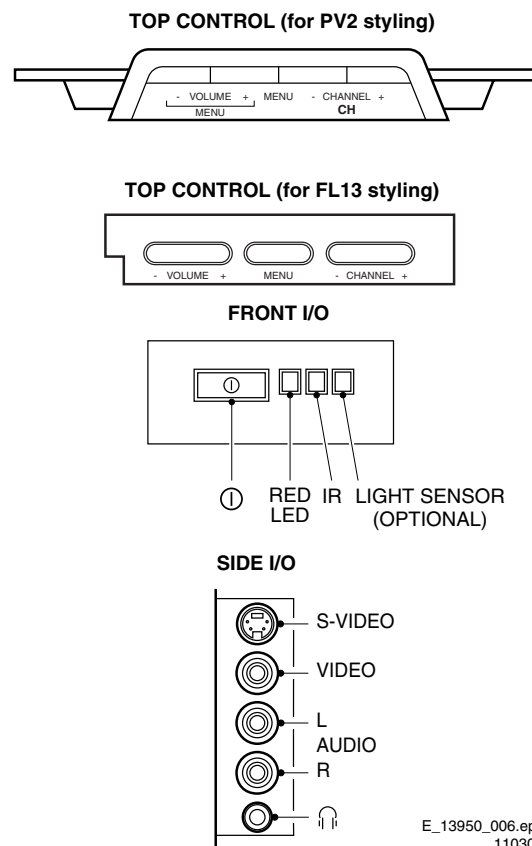


Figure 1-1 Top control and Front / Side connections

#### Hosiden: SVHS - In

1	- Y	Ground	⊥
2	- C	Ground	⊥
3	- Y	1 V <sub>pp</sub> / 75 ohm	⊕
4	- C	0.3 V <sub>pp</sub> / 75 ohm	⊕

#### Audio / Video In

Ye	- Video (CVBS)	1 V <sub>pp</sub> / 75 ohm	⊥
Wh	- Audio - L	0.2 V <sub>rms</sub> / 10 kohm	⊕ ⊕
Rd	- Audio - R	0.2 V <sub>rms</sub> / 10 kohm	⊕ ⊕

#### Mini Jack: Headphone - Out

- Headphone 32 - 600 ohm / 10 mW



## 1.2.2 Rear Connections

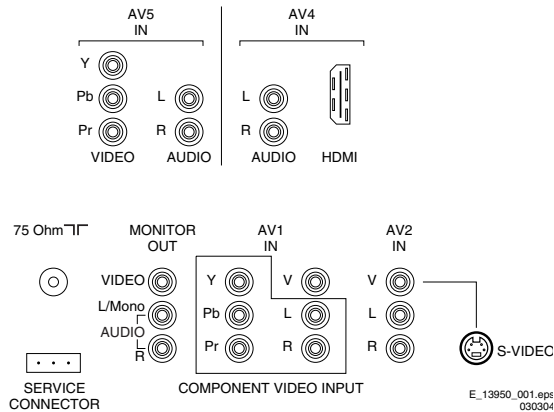


Figure 1-2 Rear connections

**Aerial In**

-F-type Coax, 75 ohm

**Monitor Out**Ye - Video (CVBS) 1 V<sub>pp</sub> / 75 ohmWh - Audio - L 0.5 V<sub>rms</sub> / 1 kohmRd - Audio - R 0.5 V<sub>rms</sub> / 1 kohm**AV1 In**Gn - Y 0.7 V<sub>pp</sub> / 75 ohmBu - Pb 0.7 V<sub>pp</sub> / 75 ohmRd - Pr 0.7 V<sub>pp</sub> / 75 ohmYe - Video (CVBS) 1 V<sub>pp</sub> / 75 ohmWh - Audio - L 0.5 V<sub>rms</sub> / 10 kohmRd - Audio - R 0.5 V<sub>rms</sub> / 10 kohm**AV2 In**Ye - Video (CVBS) 1 V<sub>pp</sub> / 75 ohmWh - Audio - L 0.5 V<sub>rms</sub> / 10 kohmRd - Audio - R 0.5 V<sub>rms</sub> / 10 kohm**AV2 In (SVHS)**

1 - Ground GND



2 - Ground GND

3 - Y 1 V<sub>pp</sub> / 75 ohm4 - C 0.3 V<sub>pp</sub> / 75 ohm**AV4 In (not used for 27/32MS series)**Wh - Audio - L 0.5 V<sub>rms</sub> / 10 kohmRd - Audio - R 0.5 V<sub>rms</sub> / 10 kohm**HDMI (not used for 27/32MS series)**

1 - RX2+ Data channel



2 - GND Ground



3 - RX2- Data channel



4 - RX1+ Data channel



5 - GND Ground



6 - RX1- Data channel



7 - RX0+ Data channel



8 - GND Ground



9 - RX0- Data channel



10 - RXC+ Data channel



11 - GND Ground



12 - RXC- Data channel



13 - n.c.

14 - n.c.

15 - DDC SCL DDC clock



16 - DDC SDA DDC data



17 - GND Ground



18 - +5V



19 - HPD



20 - GND Ground



21 - GND Ground



22 - GND Ground



23 - GND Ground



24 - GND Ground

**AV5 In**Gn - Y 0.7 V<sub>pp</sub> / 75 ohmBu - Pb 0.7 V<sub>pp</sub> / 75 ohmRd - Pr 0.7 V<sub>pp</sub> / 75 ohmWh - Audio - L 0.5 V<sub>rms</sub> / 10 kohmRd - Audio - R 0.5 V<sub>rms</sub> / 10 kohm

## 1.3 Chassis Overview

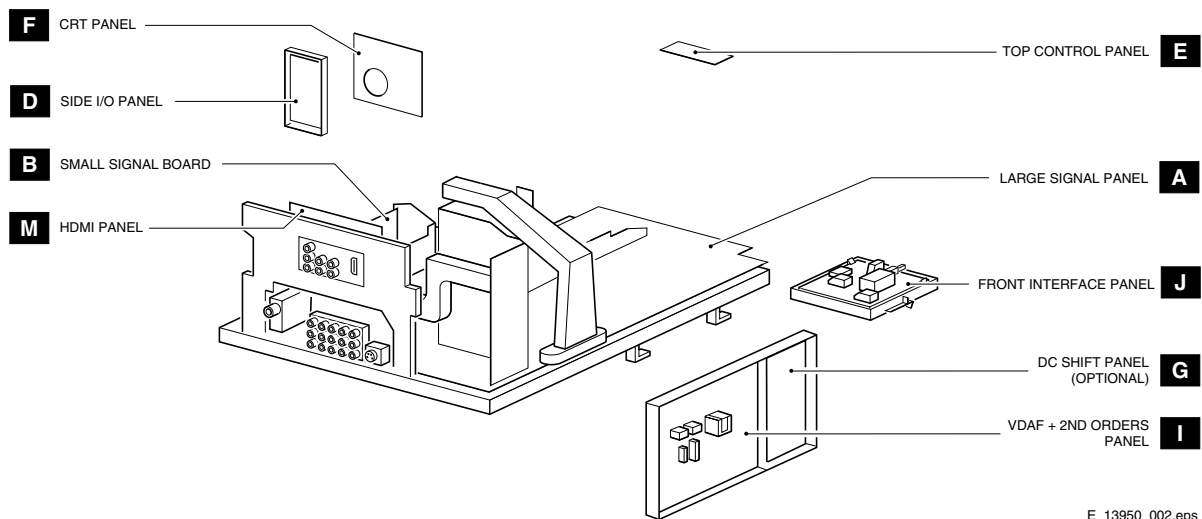

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Figure 1-3 PWB location

## 2. Safety Instructions, Warnings, and Notes

### 2.1 Safety Instructions

Safety regulations require that **during** a repair:

- Due to the chassis concept, a very large part of the circuitry (incl. deflection) is 'hot'. Therefore, connect the set to the mains via an isolation transformer.
- Replace safety components, indicated by the symbol , only by components identical to the original ones. Any other component substitution (other than original type) may increase risk of fire or electrical shock hazard.
- Wear safety goggles when you replace the CRT.

Safety regulations require that **after** a repair, you must return the set in its original condition. Pay, in particular, attention to the following points:

- General repair instruction: as a strict precaution, we advise you to re-solder the solder connections through which the horizontal deflection current is flowing. In particular this is valid for the:
  1. Pins of the line output transformer (LOT).
  2. Fly-back capacitor(s).
  3. S-correction capacitor(s).
  4. Line output transistor.
  5. Pins of the connector with wires to the deflection coil.
  6. Other components through which the deflection current flows.

**Note:** This re-soldering is advised to prevent bad connections due to metal fatigue in solder connections, and is therefore only necessary for television sets more than two years old.

- Check the insulation of the mains cord for external damage.
- Check the strain relief of the mains cord for proper function, to prevent the cord from touching the CRT, hot components, or heat sinks.
- Check the electrical DC resistance between the mains plug and the secondary side (only for sets that have an isolated power supply). Do this as follows:
  1. Unplug the mains cord and connect a wire between the two pins of the mains plug.
  2. Turn on the main power switch (keep the mains cord unplugged!).
  3. Measure the resistance value between the pins of the mains plug and the metal shielding of the tuner or the aerial connection of the set. The reading should be between 4.5 MΩ and 12 MΩ.
  4. Switch the TV 'off' and remove the wire between the two pins of the mains plug.
- Check the cabinet for defects, to prevent the possibility of the customer touching any internal parts.

### 2.2 Maintenance Instructions

We recommend a maintenance inspection carried out by qualified service personnel. The interval depends on the usage conditions:

- When a customer uses the set under normal circumstances, for example in a living room, the recommended interval is three to five years.
- When a customer uses the set in an environment with higher dust, grease, or moisture levels, for example in a kitchen, the recommended interval is one year.
- The maintenance inspection includes the following actions:
  1. Perform the 'general repair instruction' noted above.
  2. Clean the power supply and deflection circuitry on the chassis.
  3. Clean the picture tube panel and the neck of the picture tube.

### 2.3 Warnings

- In order to prevent damage to ICs and transistors, avoid all high voltage flashovers. In order to prevent damage to the picture tube, use the method shown in Fig. 2-1, to discharge the picture tube. Use a high voltage probe and a multi-meter (position V<sub>dc</sub>). Discharge until the meter reading is 0 V (after approx. 30 s).

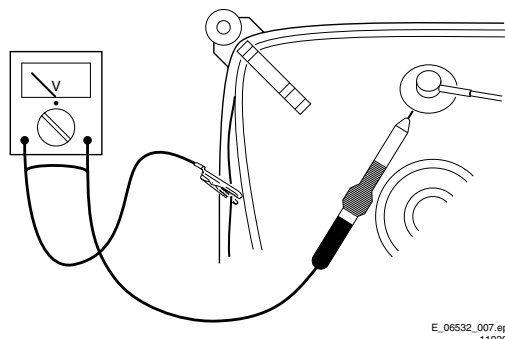









Figure 2-1 Discharge picture tube

- All ICs and many other semiconductors are susceptible to electrostatic discharges (ESD, ). Careless handling during repair can reduce life drastically. Make sure that, during repair, you are connected with the same potential as the mass of the set by a wristband with resistance. Keep components and tools also at this potential. Available ESD protection equipment:
  - Complete kit ESD3 (small tablemat, wristband, connection box, extension cable and ground cable) 4822 310 10671.
  - Wristband tester 4822 344 13999.
- Together with the deflection unit and any multi-pole unit, flat square picture tubes form an integrated unit. The deflection and the multi-pole units are set optimally at the factory. We do not recommend adjusting this unit during repair.
- Be careful during measurements in the high voltage section and on the picture tube.
- Never replace modules or other components while the unit is 'on'.
- When you align the set, use plastic rather than metal tools. This will prevent any short circuits and the danger of a circuit becoming unstable.

### 2.4 Notes

#### 2.4.1 General

- Measure the voltages and waveforms with regard to the chassis (= tuner) ground () or hot ground () depending on the tested area of circuitry.
- The voltages and waveforms shown in the diagrams are indicative. Measure them in the Service Default Mode (see chapter 5) with a color bar signal and stereo sound (L: 3 kHz, R: 1 kHz unless stated otherwise) and picture carrier at 475.25 MHz (PAL) or 61.25 MHz (NTSC, channel 3).
- Where necessary, measure the waveforms and voltages with () and without () aerial signal. Measure the voltages in the power supply section both in normal operation () and in standby (). These values are indicated by means of the appropriate symbols.
- The picture tube panel has printed spark gaps. Each spark gap is connected between an electrode of the picture tube and the Aquadag coating.



- The semiconductors indicated in the circuit diagram and in the parts lists, are interchangeable per position with the semiconductors in the unit, irrespective of the type indication on these semiconductors.
- Manufactured under license from Dolby Laboratories. 'Dolby', 'Pro Logic' and the 'double-D symbol', are trademarks of Dolby Laboratories.



Figure 2-2 Dolby Prologic

#### 2.4.2 Schematic Notes

- All resistor values are in ohms and the value multiplier is often used to indicate the decimal point location (e.g. 2K2 indicates 2.2 kohm).
- Resistor values with no multiplier may be indicated with either an "E" or an "R" (e.g. 220E or 220R indicates 220 ohm).
- All capacitor values are expressed in micro-farads ( $\mu = \times 10^{-6}$ ), nano-farads ( $n = \times 10^{-9}$ ), or pico-farads ( $p = \times 10^{-12}$ ).
- Capacitor values may also use the value multiplier as the decimal point indication (e.g. 2p2 indicates 2.2 pF).
- An "asterisk" (\*) indicates component usage varies. Refer to the diversity tables for the correct values.
- The correct component values are listed in the Electrical Replacement Parts List. Therefore, always check this list when there is any doubt.

#### 2.4.3 Rework on BGA (Ball Grid Array) ICs

##### General

Although (LF)BGA assembly yields are very high, there may still be a requirement for component rework. By rework, we mean the process of removing the component from the PWB and replacing it with a new component. If an (LF)BGA is removed from a PWB, the solder balls of the component are deformed drastically so the removed (LF)BGA has to be discarded.

##### Device removal

As is the case with any component that, it is essential when removing an (LF)BGA, the board, tracks, solder lands, or surrounding components are not damaged. To remove an (LF)BGA, the board must be uniformly heated to a temperature close to the reflow soldering temperature. A uniform temperature reduces the chance of warping the PWB. To do this, we recommend that the board is heated until it is certain that all the joints are molten. Then carefully pull the component off the board with a vacuum nozzle. For the appropriate temperature profiles, see the IC data sheet.

##### Area preparation

When the component has been removed, the vacant IC area must be cleaned before replacing the (LF)BGA. Removing an IC often leaves varying amounts of solder on the mounting lands. This excessive solder can be removed with either a solder sucker or solder wick. The remaining flux can be removed with a brush and cleaning agent. After the board is properly cleaned and inspected, apply flux on the solder lands and on the connection balls of the (LF)BGA.  
**Note:** Do not apply solder paste, as this has shown to result in problems during re-soldering.

##### Device replacement

The last step in the repair process is to solder the new component on the board. Ideally, the (LF)BGA should be aligned under a microscope or magnifying glass. If this is not possible, try to align the (LF)BGA with any board markers.

To reflow the solder, apply a temperature profile according to the *IC data sheet*. So as not to damage neighboring components, it may be necessary to reduce some temperatures and times.

#### 2.4.4 Practical Service Precautions

- **It makes sense to avoid exposure to electrical shock.** While some sources are expected to have a possible dangerous impact, others of quite high potential are of limited current and are sometimes held in less regard.
- **Always respect voltages.** While some may not be dangerous in themselves, they can cause unexpected reactions - reactions that are best avoided. Before reaching into a powered TV set, it is best to test the high voltage insulation. It is easy to do, and is a good service precaution.
- **Before powering up the TV set with the back cover off** (or on a test fixture), attach a clip lead to the CRT DAG ground and to a screwdriver blade that has a well insulated handle. After the TV is powered "on" and high voltage has developed, probe the anode lead with the blade, starting at the case of the High Voltage Transformer (flyback - IFT). Move the blade to within two inches of the connector of the CRT. **If there is an arc, you found it the easy way, without getting a shock!** If there is an arc to the screwdriver blade, replace the part that is causing the problem; the High Voltage Transformer or the lead (if it is removable)





## 4. Mechanical Instructions

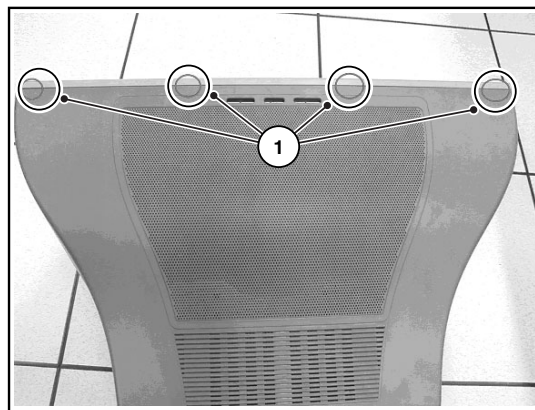
Index of this chapter:

1. Service connector
2. Set Disassembly
3. Service Positions
4. Assies / Panels Removal
5. Set Reassembly

**Note:** figures below can deviate slightly from the actual situation, due to the different set executions.

### 4.1 Service Connector (for ComPair)

For service diagnostics with ComPair, it is not necessary to disassemble the set. You only have to connect the ComPair interface box via the appropriate cable, to the service connector on the rear of the set (see figure "Rear connections" in chapter "Technical specifications, ..."), and start the program (see also chapter "Service Modes ....").



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Figure 4-2 Rear cover (for FL13 styling)

### 4.2 Set Disassembly

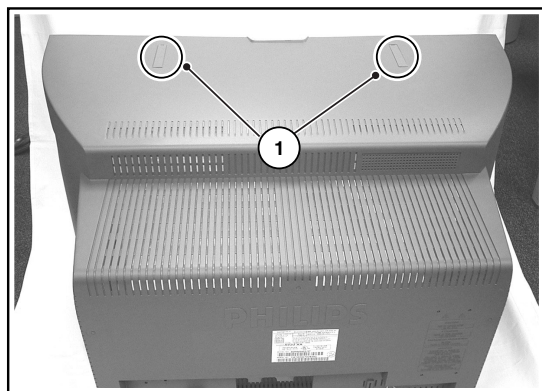
Follow the disassemble instructions in described order.

#### 4.2.1 Rear Cover Removal

**Warning:** disconnect the mains power cord before you remove the rear cover.

**For PV2 styling (for 8402 and 8302 sets)**

1. Manually unlock and remove the two plastic cover cups (1) (if present) on the top of TV.
2. Remove all the fixation screws of the rear cover.
3. Remove the rear cover.



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Figure 4-1 Rear cover (for PV2 styling)

**For FL13 styling (for 8502 sets)**

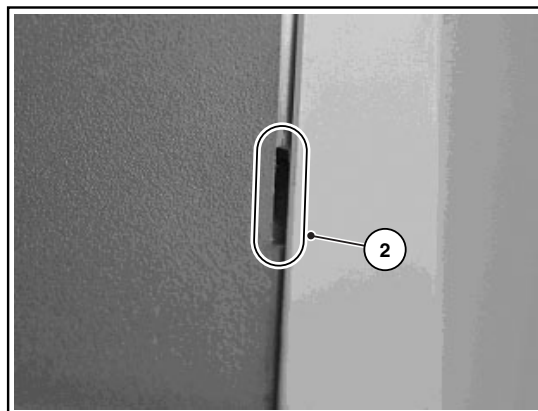
1. Remove all screws. If you do not remove them, you cannot access the clips.
2. Tilt the set a little forward, so that you can release the two clickfit clamps that are located at the bottomplate of the set.
3. Four openings (1) can be found at the top. The openings are very small (2).

**Note:** Some sets only have the two inner openings.

4. Underneath every opening there is a clip. Push this clip down with a very thin piece of metal (3), until you hear a click.

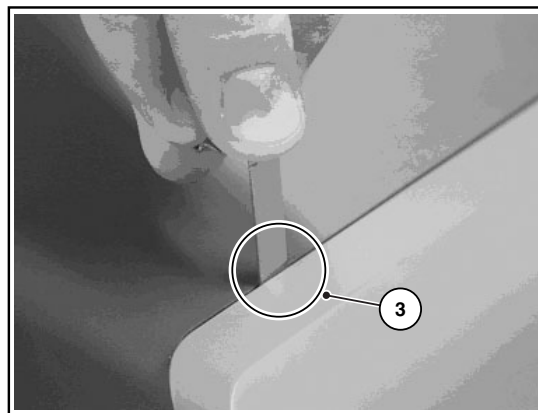
**Caution:** do **not** use a screwdriver, this will damage the cabinet.

5. When all four clips are pushed down, the back cover can be removed.



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Figure 4-3 Opening



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Figure 4-4 Pushing clips down



### 4.3 Service Positions

This chassis has several predefined service positions, for better accessibility. They are explained below in more detail.

#### 4.3.1 Large Signal Panel (LSP)

##### **Service position 1 - Component Side of the LSP**

For better accessibility of the LSP, do the following (see Figure "Service position 1"):

1. Remove the LSP-bracket from the bottom tray by pulling it backwards.
2. Hook the bracket in the first row of fixation holes of the bottom tray. In other words, reposition the bracket from (1) to (2).

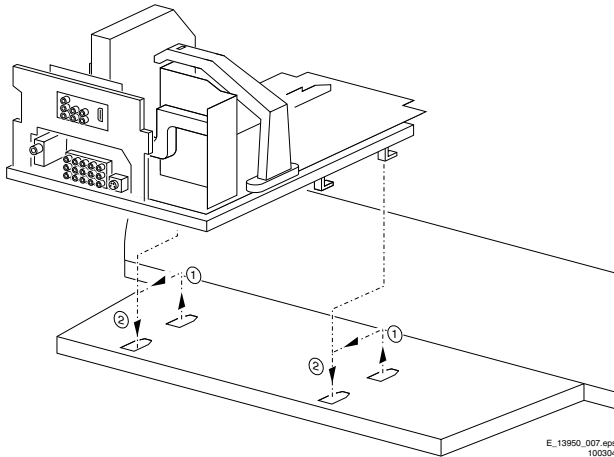


Figure 4-5 Service position 1

##### **Service position 2 - Solder Side of the LSP**

To get access to the bottom side (solder side) of the LSP, do the following (see figure above):

1. Remove the DC-Shift assy (1) (see paragraph "DC-Shift Assy/Panel" below).
2. Release the Front interface assy from the bottom plate (2) (see paragraph "Top Control Assy/Panel" below).
3. Disconnect the degaussing coil from the LSP. Therefore remove the cable from the connector 1502.
4. Release some wiring from their fixation clamps, in order to get room for repositioning the LSP.
5. Flip the LSP 90 degrees clockwise (3), and place it vertically on the bottom plate and a table.

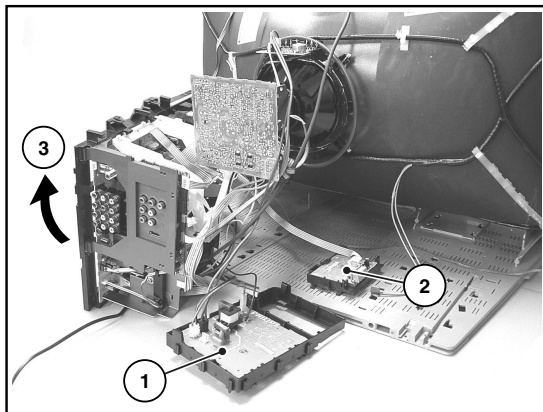


Figure 4-6 Service position 2

### 4.4 Assies/Panels Removal

Sometimes, it can be necessary to swap a complete assy or Printed Wiring Board (PWB). How that can be done is explained below.

#### 4.4.1 Top Control Assy/Panel

1. Remove the two fixation screws:
  - PV2 styling: assy is mounted into the front cabinet;
  - FL13 styling: assy is mounted into the rear cover.
2. Push the assy a little bit upwards, and then pull it backwards to release it from the front hinge.
3. Lift the panel from its bracket, while releasing the four fixation clamps.

#### 4.4.2 Side I/O Assy and Panel

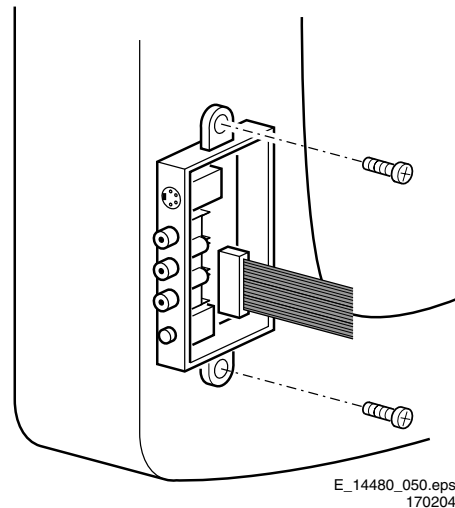


Figure 4-7 Side-I/O assy/panel

1. Remove the two fixation screws, and remove the complete Side I/O assembly.
2. Release the two fixation clamps, and lift the panel from the bracket.

#### 4.4.3 HDMI Assy/Panel Removal

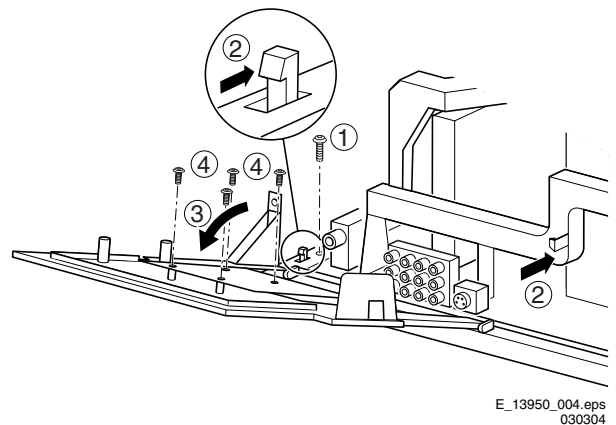
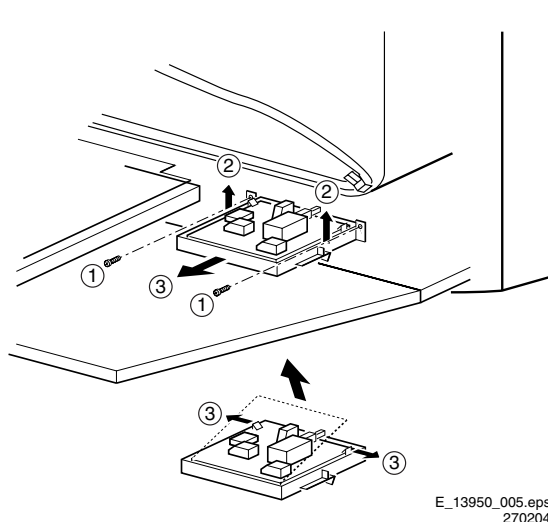


Figure 4-8 HDMI assy/panel

1. Remove the fixation screw (1) (if present).
2. Release the two pegs (2), by pushing them towards CRT.
3. At the same time, pull the complete module away from the LSP bracket (3). It hinges in the LSP bracket.
4. Remove the four fixing screws (4), and remove the panel.

#### 4.4.4 Front Interface Assy/Panel

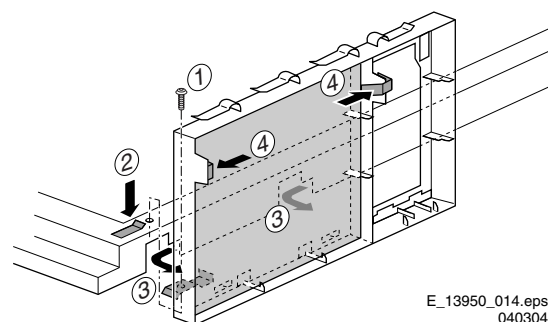


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Figure 4-9 Front Interface assy/panel

1. Remove the two fixation screws (1).
2. Remove the complete module from the bottom plate, by pulling the two fixation clamps upward (2), while sliding the module away from the CRT (3).
3. Release the two clamps (4) at the sides of the bracket and lift panel out (it hinges at one side).

#### 4.4.5 VDAF Assy/Panel



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Figure 4-10 VDAF assy/panel

1. Remove the fixation screw (1) (if present).
2. Push down the fixation clamp (2), and pull the complete bracket at the same time away from the CRT (3). The module is now free from the LSP-bracket.
3. Release the two clamps (4) at the sides of the bracket and lift panel out.

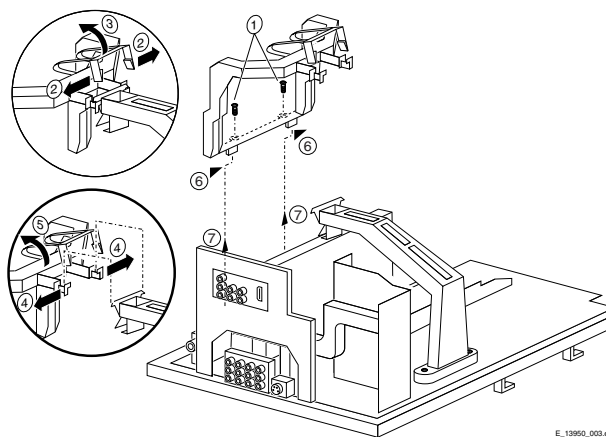
#### 4.4.6 Small Signal Board (SSB)

In fact, there is no predefined service position for the SSB. Most test points are located on the A-side (side that is facing the tuner).

If you have to replace ICs, you must take the complete SSB module out of the SIMM-connector.

To get access to the SSB test points, do the following:

1. Put the LSP in service position 1 (as described above).
2. Remove the fixation screws, which hold the SSB-bracket (1).
3. Release the clamping jaw at the top of the SSB bracket (2) and (3).
4. Push the two clamping lugs outwards, and pull the top of the bracket at the same time upwards (4) and (5).
5. Now you can remove the complete bracket. Push it, at the height of the LSP-bracket, towards the CRT (6) and lift it out of the LSP-bracket (7).
6. Take the SSB out, disconnecting it from the LSP.



E\_13950\_003.eps  
030304

Figure 4-11 Small signal board

#### Notes:

- For better access to the SSB, it is possible to order an "extension tool" with cables. You can use this service extension tool to connect a Small Signal Board (SSB) of an Axx or EMx chassis, via two "IDE" cables to the SIMM connector in the set. In this way, you can service the SSB more easily outside the TV set. You can order this tool under 12nc: 9965 000 14526.
- If necessary for the measurement, you can put the LSP in the "service position 2" (as described above).

#### 4.4.7 Large Signal Panel (LSP)

1. Remove the HDMI assy (see paragraph "HDMI assy/panel" above).
2. Remove the SSB (see paragraph "Small Signal Board (SSB)" above).
3. Disconnect the necessary cables.
4. Remove the fixation screw, which is located nearby the SIMM-connector.
5. Release the fixation clamps on the left of the LSP-bracket (the panel hinges at the right side).
6. Remove the panel from the bracket.

### 4.5 Set Re-assembly

To re-assemble the whole set, do all processes in reverse order.

**Note:** be sure that, before the rear cover is mounted:

- The mains cord is mounted correctly in its guiding brackets.
- All wires/cables are returned in their original positions. This is very important due to the large "hot" area of the set

## 5. Service Modes, Error Codes, and Fault Finding

Index of this chapter:

1. Test points
2. Service Modes
3. Problems and solving tips (related to CSM)
4. ComPair
5. Error Codes
6. The blinking LED procedure
7. Protections
8. Repair tips
9. Software downloading

### 5.1 Test Points

See chapter 6 "Block Diagrams, Test point Overview, and Waveforms".

Perform measurements under the following conditions:

- Service Default Mode.
- Video: color bar signal.
- Audio: 3 kHz left, 1 kHz right.

### 5.2 Service Modes

Service Default Mode (SDM) and Service Alignment Mode (SAM) offer several features for the service technician, while the Customer Service Mode (CSM) is used for communication between a Philips Customer Care Center (P3C) and a customer.

There is also the option of using ComPair, a hardware interface between a computer (see requirements below) and the TV chassis. It offers the ability of structured troubleshooting, test pattern generation, error code reading, software version readout, and software upgrading.

**Minimum requirements:** a Pentium processor, Windows 95/98, and a CD-ROM drive (see also paragraph "ComPair").

#### 5.2.1 Service Default Mode (SDM)

##### **Purpose**

- To create a pre-defined setting, to get the same measurement results as given in this manual.
- To override SW protections (only when SDM is entered via shorting the SDM pins on the SSB).
- To start the blinking LED procedure.
- Inspection of error buffer, life timer, and software version.

##### **Specifications**

- Tuning frequency: 61.25 MHz (channel 3).
- Color system: NTSC M.
- All picture settings at 50 % (brightness, color, contrast).
- All sound settings at 50 %, except volume at 25 %.
- All service-unfriendly modes (if present) are disabled, like:
  - (Sleep) timer.
  - Child/parental lock.
  - Blue mute.
  - Automatic volume limiter (AVL).
  - Auto switch-off (when no video signal was received for 10 minutes).
  - Skip/blank of non-favorite pre-sets.
  - Hotel or hospital mode.
  - Local keyboard block.
  - Smart modes.
  - Auto store of personal presets.
  - Auto user menu time-out.

#### 5.2.2 Service Alignment Mode (SAM)

##### **Purpose**

##### **How to enter SDM**

Use one of the following methods:

- Use the standard RC-transmitter and key in the code "062596", directly followed by the "MENU" button.  
**Note:** It is possible that, together with the SDM, the main menu will appear. To switch it "off", push the "MENU" button again.
- Short circuit, during switch "on" of the set, the two solder pads on the SSB with the indication "FOR SERVICE". These solder pads are located at the "tuner" side of the SSB (just above the large BGA IC).  
**Caution:** If the SDM is entered via these pins, all the software-controlled protections are de-activated for 15 s. When these 15 s are expired, the set will shutdown to protection mode.
- Use the DST-emulation feature of ComPair.
- Use the "DEFAULT" button on the Dealer Service Tool (RC7150).

After entering this mode:

- "SDM" will appear in the upper right corner of the screen.
- Also, the error buffer, operating hours, and software version are displayed (can be toggled "on/off" with the "STATUS / OSD / [i+]" button).
- Blinking LED procedure will be started.
- All software-controlled protections are overridden for 15 s. When these 15 s are expired, the set will shutdown to protection mode.

##### **Contents of SDM:**

- **HRS.** Displays the accumulated total of operation hours (not the standby hours) in a hexadecimal value.
- **SW ID.** Displays the date of the software and the software version of the ROM  
**Example:** A02EB1\_1.00 = AAABBC-X.YY.  
 – **AAA**= chassis name.  
 – **BB**= region and/or function name: E= Europe, A= Asia Pacific, U= NAFTA, L= LATAM, B= Basic, T= Top, P= PAL, N= NTSC, S= Stereo, M= Mono.  
 – **C**= the language cluster number.  
 – **X.Y**= the software version, where X is the main version number (different numbers are not compatible with one another) and Y is the sub version number (a higher number is always compatible with a lower number).
- **ERR** (followed by maximal 8 errors). The most recent error is displayed at the upper left (for an error explanation see paragraph "Error Codes").

##### **How to navigate**

- When you press the "MENU" button on the RC transmitter, the set will toggle between the SDM and the normal user menu (with the SDM mode still active in the background).
- When you press the "STATUS" button on the RC transmitter, the set will toggle only display "SDM". This mode is useful when performing measurements, then the OSD info will not generate interference.

##### **How to exit SDM**

Use one of the following methods:

- Switch the set to STANDBY via a standard customer RC-transmitter (the error buffer is erased).
- Via a standard customer RC-transmitter: key in "00"-sequence (the error buffer is **not** erased).
- To perform alignments.
- To change option settings.
- To easily identify the used software version.



- To view operation hours.
- To display / clear the error code buffer.

### Specifications

- Operating hours counter.
- Software version.
- Option settings.
- Error buffer reading and erasing.
- Software alignments.
- Disable service unfriendly modes.

### How to enter SAM

Use one of the following methods:

- Via a standard RC transmitter: key in the code "062596" directly followed by the "STATUS" button.
- Use the DST-emulation feature of ComPair.
- Press the "ALIGN" button on the DST while the set is in the normal operation

After entering this mode, "SAM" will appear in the upper right corner of the screen.

### Contents of SAM:

- **HRS.** Displays the accumulated total of operation hours (not the standby hours) in a hexadecimal value  
**Note:** every time the set is switched "on" by the AC power switch or the RC, the timer is increased by 0.5.
- **SW ID.** Displays the date of the software and the software version of the ROM (**example:** A02UB1-1.00 = AAABBC-X.YY).
  - **AAA**= chassis name.
  - **BB**= region and/or function name: E= Europe, A= Asia Pacific, U= NAFTA, L= LATAM, B= Basic, T= Top, P= PAL, N= NTSC, S= Stereo, M= Mono.
  - **C**= the language cluster number.
  - **X.Y**= the software version, where X is the main version number (different numbers are not compatible with one another) and Y is the sub version number (a higher number is always compatible with a lower number).
- **ERR** (followed by maximal 8 errors). The most recent error is displayed at the upper left (for an error explanation see paragraph "Error Codes").
- **OPTIONS.** Extra feature for Service to set the Option Codes.
- **CLEAR ERRORS.** When you press the "OK" button, the error buffer is reset.
- **AKB.** Disable (off) or enable (on) the "black current loop" (AKB= Auto Kine Bias). For Vg2 alignment.
- **TUNER.** This will activate the "TUNER" alignments sub-menu.
- **WHITE TONE.** This will activate the "WHITE TONE" alignments sub-menu.
- **GEOMETRY.** This will activate the "GEOMETRY" alignments sub-menu.
- **SOUND.** This will activate the "SOUND" alignments sub-menu.
- **SMART SETTINGS.** This will activate the "SMART SETTINGS" alignments sub-menu.
- **STORE.** This will save the new settings/alignments.
- **EEPROM TEST.** This will report if the SW checksum is OK. Convenient after SW upgrading.
- **VID RAM TEST.** This will check the continuity of the address bus and data bus of the Video RAM.
- **VG2.** This feature is not implemented yet. Do not use.

**Note:** Alignments are described in chapter 8 "Alignments".

### How to navigate

- In SAM, you can select the menu items with the "CURSOR UP/DOWN" key on the RC-transmitter. The selected item will be highlighted. When not all menu items fit on the screen, move the "CURSOR UP/DOWN" key to display the next/previous menu items.
- With the "CURSOR LEFT/RIGHT" keys, it is possible to:

- (De) activate the selected menu item.
- Change the value of the selected menu item.
- Activate the selected submenu.
- When you press the "MENU" button on the RC transmitter, the set will toggle between the SAM and the normal user menu (with the SAM mode still active in the background).

### How to exit SAM

Use one of the following methods:

- Switch the set to STANDBY via the RC-transmitter (the error buffer is erased).
- Via a standard customer RC-transmitter: key in "00"-sequence (the error buffer is **not** erased).

## 5.2.3 Customer Service Mode (CSM)

### Purpose

When a customer is having problems with his TV-set, he can call his dealer or the Philips helpdesk (P3C). The service technician can then ask the customer to activate the CSM, in order to identify the status of the set. Now, the service technician can judge the severity of the complaint. In many cases, he can advise the customer how to solve the problem, or he can decide if it is necessary to visit the customer. The CSM is a **read only** mode; therefore, modifications in this mode are not possible.

### How to enter CSM

Key in the code "123654" via the standard RC transmitter.

**Note:** set must be in "Widescreen" mode (via button "PIC SIZE" on the remote control)

### Notes:

- Activation of the CSM is only possible if there is no (user) menu on the screen!
- During CSM, sound volume is set to 25% of the scale, "Smart Sound" is set to "Theatre" mode, and "Smart Picture" is set to "Rich/Movies" mode temporarily to ensure a good picture and sound of the working set. After leaving CSM, the original settings are restored.

### How to navigate

By means of the "CURSOR-DOWN/UP" knob on the RC-transmitter, you can navigate through the menus.

### Contents of CSM

The following information is displayed on screen:

- Text "CSM" on the first line.
- Line number for every line (to make CSM language independent).
- Option code information.
- Configuration information.
- Service-unfriendly modes.

### CSM 1

1. **SET TYPE** (if displayed). Type/model number according to the Philips standard.
2. **SOFTWARE.** Software version AAABBC-X.YY.
3. **HOURS ON.** Operating hours (in hexadecimal).
4. **CODE 1.** Shows the contents of the error buffer (the word "error" may not be used on this screen, instead "codes" is used).
5. **CODE 2.** Shows the contents of the error buffer (the word "error" may not be used on this screen, instead "codes" is used).
6. **OPTION 1.** Option code information (for more details see chapter 8 "Alignments").
7. **OPTION 2.** Option code information (for more details see chapter 8 "Alignments").
8. **OPTION 3.** Option code information (for more details see chapter 8 "Alignments").
9. **OPTION 4.** Option code information (for more details see chapter 8 "Alignments").

10. **SIGNAL.** State of the "ident" signal.
11. **TIMER** (if present). State of the timer (in "FEATURE" menu).

**CSM 2**

1. **CHANNEL** (if present). State of the Child Lock.
2. **PRESET** (if present). State of the Current channel.
3. **HOTELMODE** (if present). Shows if the HOTEL mode is activated.
4. **SOURCE.** Selected source before entry of CSM.
5. **SOUND.** Selected SOUND mode prior entry to CSM.
6. **VOLUME.** Volume level before entry of CSM.
7. **BALANCE.** Balance level before entry of CSM.
8. **BRIGHTNESS.** Brightness level before entry of CSM.
9. **COLOR.** Color level before entry of CSM.
10. **CONTRAST.** Contrast level before entry of CSM.
11. **HUE** (if present). Hue level before entry of CSM.

**How to exit CSM**

Use one of the following methods:

- After you press a key on the RC-transmitter (with exception of the "CHANNEL", "VOLUME" and digit (0-9) keys), or
- After you switch the TV-set "off" with the AC power switch.
- After 15 min. no RC or local keyboard actions.

**5.3 Problems and Solving Tips (related to CSM)**

**Note:** Below described problems are all related to the TV settings. The procedures to change the value (or status) of the different settings are described above. New value(s) are automatically stored.

**5.3.1 Picture Problems****Picture too dark**

1. Press SMART PICTURE several times on the RC. In case the picture improves, increase the "Brightness" or the "Contrast" value.
2. Check in CSM lines BRIGHTNESS and/or CONTRAST. If the value of line BRIGHTNESS is low (< 10) or the value of line CONTRAST is low (< 10), increase them. The new value(s) are automatically stored (in "personal" pre-set) for all TV channels.

**Picture too bright**

1. Press SMART PICTURE several times on the RC. In case the picture improves, decrease the "Brightness" or the "Contrast" value.
2. Check in CSM lines BRIGHTNESS and/or CONTRAST. If the value of line BRIGHTNESS is high (> 40) or the value of line CONTRAST is high (> 50), decrease the "Brightness" or the "Contrast" value. The new value(s) are automatically stored (in "personal" pre-set) for all TV channels.

**White line around picture elements and text**

1. Press SMART PICTURE several times on the RC. In case the picture improves, decrease the "Sharpness" value.
2. Check in CSM line SHARPNESS. Decrease the "Sharpness" value. The new value is automatically stored for all TV channels. The new value is automatically stored (in "personal" pre-set) for all TV channels.

**No picture**

Check in CSM line 7. In case this line shows NO SIGNAL, check the aerial cable/aerial system.

**Blue picture**

No proper signal is received. Check the aerial cable/aerial system.

**Blue picture and/or unstable picture**

A scrambled or decoded signal is received.

**Black and white picture**

Check in CSM line COLOR. In case the value is low (< 10), increase the "Color" value. The new value is automatically stored for all TV channels.

**No colors/color lines around picture elements or colors not correct or unstable picture**

1. Check in CSM line SYSTEM. If a "strange" system pops up, something has gone wrong during installation. Re-install the channel.

**Menu text not sharp enough**

1. Press "SMART PICTURE". In case picture improves, decrease the "Contrast" value. The new value(s) are automatically stored for all TV channels.
2. Check in CSM line CONTRAST. If the value of this line is high (> 50), decrease the "Contrast" value.

**5.3.2 Sound Problems****No sound from left and right speaker**

Check in CSM line VOLUME. If the value is low, increase the value of "Volume". The new value(s) are automatically stored (in "personal" pre-set) for all TV channels.

**Sound too loud for left and right speaker**

Check in CSM line VOLUME. If the value is low, decrease the value of "Volume". The new value(s) are automatically stored (in "personal" pre-set) for all TV channels.

**5.4 ComPair****5.4.1 Introduction**

ComPair (Computer Aided Repair) is a service tool for Philips Consumer Electronics products. ComPair is a further development on the European DST (service remote control), which allows faster and more accurate diagnostics. ComPair has three big advantages:

ComPair helps you to quickly get an understanding on how to repair the chassis in a short time by guiding you systematically through the repair procedures.

ComPair allows very detailed diagnostics (on I2C level) and is therefore capable of accurately indicating problem areas. You do not have to know anything about I2C commands yourself because ComPair takes care of this.

ComPair speeds up the repair time since it can automatically communicate with the chassis (when the microprocessor is working) and all repair information is directly available. When ComPair is installed together with the SearchMan electronic manual of the defective chassis, schematics and PWBs are only a mouse click away.

**5.4.2 Specifications**

ComPair consists of a Windows based faultfinding program and an interface box between PC and the (defective) product. The ComPair interface box is connected to the PC via a serial (or RS232) cable.

For this chassis, the ComPair interface box and the TV communicate via a bi-directional service cable via the service connector.

The ComPair faultfinding program is able to determine the problem of the defective television. ComPair can gather diagnostic information in two ways:

- **Automatic** (by communication with the television):  
ComPair can automatically read out the contents of the entire error buffer. Diagnosis is done on I2C level. ComPair

can access the I2C bus of the television. ComPair can send and receive I2C commands to the micro controller of the television. In this way, it is possible for ComPair to communicate (read and write) to devices on the I2C busses of the TV-set.

- **Manually** (by asking questions to you): Automatic diagnosis is only possible if the micro controller of the television is working correctly and only to a certain extent. When this is not the case, ComPair will guide you through the faultfinding tree by asking you questions (e.g. Does the screen give a picture? Click on the correct answer: YES / NO) and showing you examples (e.g. Measure test-point I7 and click on the correct oscillogram you see on the oscilloscope). You can answer by clicking on a link (e.g. text or a waveform picture) that will bring you to the next step in the faultfinding process.

By a combination of automatic diagnostics and an interactive question / answer procedure, ComPair will enable you to find most problems in a fast and effective way.

Beside fault finding, ComPair provides some **additional features** like:

- Up- or downloading of pre-sets.
- Managing of pre-set lists.
- Emulation of the Dealer Service Tool (DST).
- If both ComPair and SearchMan (Electronic Service Manual) are installed, all the schematics and the PWBs of the set are available by clicking on the appropriate hyperlink.

**Example:** Measure the DC-voltage on capacitor C2568 (Schematic/Panel) at the Mono-carrier.

- Click on the "Panel" hyperlink to automatically show the PWB with a highlighted capacitor C2568.
- Click on the "Schematic" hyperlink to automatically show the position of the highlighted capacitor.

#### 5.4.3 Stepwise Start-up

This is realized via ComPair and is very helpful when a **protection** is activated (see also chapter "Protections"). Under normal circumstances, a fault in the power supply, or an error during start-up, will switch the television to protection mode. ComPair can take over the initialization of the television. In this way, it is possible to distinguish which part of the start-up routine (hence which circuitry) is causing the problem. Take notice that the transition between two steps can take some time, so give the set some time to reach a stable state. During the transition time, the LED can blink strangely.

On entering Service mode, protections and other errors can be trapped by powering the TV in stepwise fashion as explained below. The "stepwise start-up" mode is done in the specified sequence. Before entering this mode, all the protections are disabled and are only enabled step-by-step, to trap the errors more appropriately.

The following steps are involved.

##### Step 0: Standby.

- Pre-condition: The set is in protection mode.
- Post-condition: The set is switched to the stepwise start-up mode. Only the necessary Standby Supply is present, all other supplies are switched "off".

##### Step 1: Power "on".

- Pre-condition: All protections are disabled, sound amplifiers are muted, and general initialization is done.
- Post-condition: 8V and 5V supplies are "on". Degaussing is "on" and switched "off" after 3 s. The supply fault protections are enabled.

##### Step 2: Initialized.

- Pre-condition: Step 1 is done. No supply protection faults are detected.
- Post-condition: ADOC, MPIF, and Tuner components are initialized.

##### Step 3: Deflection "on".

- Pre-condition: Step 2 is done. No protection faults detected.
- Post-condition: Deflection is switched "on". The horizontal deflection fault protections are enabled.

##### Step 4: TV "on".

- Pre-condition: Step 3 is done. No protection faults detected.
- Post-condition: Picture tube is switched "on". Sound amplifiers are demuted. The X-ray/beam current fault protections are enabled.

**Note:** When the set is in stepwise mode and, due to stepping-up, a protection is activated, the set will really go into protection (blinking LED). The set will not leave the stepwise-mode however. If state X is the state where the set went to protection, stepwise start-up will return to state X-1. At state (X-1) diagnostic measurements can be performed. Also, in the short time, the set is in state X but not in protection, you can also do some measurements.

#### 5.4.4 How To Connect

1. First, install the ComPair Browser software (see the Quick Reference Card for installation instructions).
2. Connect the RS232 interface cable between a free serial (COM) port of your PC and the PC connector (marked with "PC") of the ComPair interface.
3. Connect the AC power adapter to the supply connector (marked with "POWER 9V DC") of the ComPair interface.
4. Switch the ComPair interface "off".
5. Switch the television set "off" with the AC power switch.
6. Connect the ComPair interface cable between the connector on the rear side of the ComPair interface (marked with "I2C") and the ComPair connector at the rear side of the TV (for its location see figure "Top view LSP" in chapter "Alignments").
7. Plug the AC power adapter in a AC power outlet, and switch the interface "on". The green and red LEDs light up together. The red LED extinguishes after approx. 1 second while the green LED remains lit.
8. Start the ComPair program and read the "Introduction" chapter.

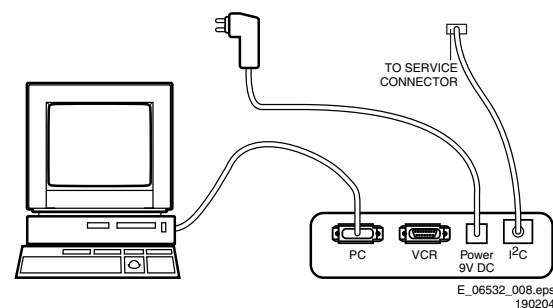


Figure 5-1 ComPair Interface connection

### 5.4.5 How To Order

ComPair order codes:

- ComPair Software: ST4191.
- ComPair Interface Box: 4822 727 21631.
- AC Adapter: T405-ND.
- ComPair Quick Start Guide: ST4190.

**Note:** If you encounter any problems, contact your local support desk.

## 5.5 Error Codes

### 5.5.1 Introduction

The error code buffer contains all detected errors since the last time the buffer was erased. The buffer is written from left to right, new errors are logged at the left side, and all other errors shift one position to the right.

When an error has occurred, the error is added to the list of errors, provided the list is not full or the error is a protection error.

When an error occurs and the error buffer is full, then the new error is not added, and the error buffer stays intact (history is maintained), except when the error is a protection error.

To prevent that an occasional error stays in the list forever, the error is removed from the list after 50+ operation hours.

When multiple errors occur (errors occurred within a short time span), there is a high probability that there is some relation between them.

### 5.5.2 How to read the Error Buffer

Use one of the following methods:

- On screen via the SAM (only if you have a picture).  
Examples:
  - **0 0 0 0**: No errors detected
  - **6 0 0 0**: Error code 6 is the last and only detected error
  - **9 6 0 0**: Error code 6 was first detected and error code 9 is the last detected error
- Via the blinking LED procedure (when you have no picture). See next paragraph.
- Via ComPair.

### 5.5.3 How to clear the Error Buffer

Use **one** of the following methods:

- By activation of the "CLEAR ERRORS" command in the SAM menu.
- With a normal RC, key in sequence "MUTE" followed by "062599" and "OK".
- When you transmit the commands "DIAGNOSE" - "99" - "OK" with ComPair (or with a DST).
- If the content of the error buffer has not changed for 50+ hours, it resets automatically.

### 5.5.4 Error Codes

Error codes are required to indicate failures in the TV set. In principle a unique error is available for every:

- I2C device error.
- I2C bus error (for every bus containing two or more I2C devices).
- Protection error (e.g. +8V protection or Horizontal protection).
- Error not related to an I2C device, but of importance (e.g. BC-loop, RAM error).

Table 5-1 Error Code Table

Error	Description
0	No error
1	Horizontal Protection (via NOHFB bit in ADOC)
3	+8V error (missing/protection active by checking MPIF ASUP bit))
4	X-ray/High beam current protection signal (via XPROT bit in ADOC)
5	Hardware Protection is active
7	Under-voltage protection
11	MPIF I2C communication failure / MPIF test failed
12	BC-loop not stabilised within the time limit (i.e. after timer is expired)
13	NVM I2C communication failure
14	Main tuner I2C failure UV13xx
15	HDMI Panel Link Receiver
17	3D Combfilter I2C communication failure
18	PIP Tuner I2C failure
21	PIP IF demodulator IC TDA988x communication failed (only for PIP/DW sets)
22	Flash over protection error (to register CRT flash-overs, via FPR bit in ADOC)

#### Service tips:

- In case of non-intermittent faults, clear the error buffer before you begin the repair. This to ensure that old error codes are no longer present. Before clearing the buffer, write down the content, as this history can give you significant information.
- If possible, check the entire contents of the error buffer. In some situations, an error code is only the result of another error code and not the actual cause (e.g., a fault in the protection detection circuitry can also lead to a protection).

## 5.6 The Blinking LED Procedure

### 5.6.1 Introduction

Via this procedure, you can make the contents of the error buffer visible via the front LED. This is especially useful for fault finding, when there is no picture.

When the SDM is entered, the front LED will show (blink) the contents of the error-buffer. Error-codes > 10 are shown as follows:

1. A long blink of 750 ms (which is an indication of the decimal digit),
2. A pause of 1500 ms,
3. "n" short blinks (where "n" = 1 - 9),
4. When all the error-codes are displayed, the sequence finishes with a LED blink of 3000 ms,
5. The sequence starts again.

**Example:** Error 12 9 6 0 0.

After activation of the SDM, the front LED will show:

1. 1 long blink of 750 ms (which is an indication of the decimal digit) followed by a pause of 1500 ms,
2. 2 short blinks of 250 ms, followed by a pause of 3000 ms,
3. 9 short blinks of 250 ms, followed by a pause of 3000 ms,
4. 6 short blinks of 250 ms, followed by a pause of 3000 ms,
5. 1 long blink of 3000 ms to finish the sequence,
6. The sequence starts again.

### 5.6.2 How to Enter

Use one of the following methods:

- Enter the SDM (only via soldering pads marked "FOR SERVICE" on the SSB). The blinking front LED will show the entire contents of the error buffer (this works in "normal operation" mode and in "protection" mode). In order to avoid confusion with RC5 signal reception blinking, this LED blinking procedure is terminated when an RC5 command is received.
- Transmit the commands "MUTE", "06250x", and "OK" with a normal RC (where "x" is the position in the error buffer that has to be displayed). With x= 1, the last detected error is shown, x= 2 the second last error, etc.... When x= 0, all errors are shown.
- "DIAGNOSE X" with the DST (where "x" is the position in the error buffer that has to be displayed). With x= 1, the last detected error is shown, x= 2 the second last error, etc.... When x= 0, all errors are shown.

**Note:** It can take some seconds before the blinking LED starts.

## 5.7 Protections

### 5.7.1 Introduction

Fault protections are introduced to avoid unacceptable temperature rising and burning hazards. If a fault situation is detected, an error code will be generated and if necessary, the set is put in protection mode.

The protection mode is indicated by the blinking of the front LED at a frequency of 3 Hz (or by a coded blinking in special cases). For the customer, it is made impossible to switch "on" the set during a protection.

It is possible to determine the type of fault by interpreting the blinking pattern of the LED indicator. It is also possible to read out the error codes from the NVM via ComPair. It is possible to de-activate the protection states in Service Default Mode.

The following protections are implemented:

**Table 5-2 Protections overview**

Protection	Detection method	Bit name	Detection
Under Voltage	Via ADC (KB)	ADC (KB)	ADC input
+8V Supply	Via MPIF_IRQ	ASUP	MPIF internal register
Horizontal fly-back	Via interrupts	NOHFB	ADOC internal register (DOP)
X-ray	Via interrupts	XPROT	ADOC internal register (DOP)
Beam Current	Via interrupts	BCF	ADOC internal register (DOP)
Flash	Hardware ctrl	-	Hardware
Arc	Hardware ctrl	-	Hardware
Vertical	Hardware ctrl	-	Hardware
East/West	Hardware ctrl	-	Hardware
Bridge coil	Hardware ctrl	-	Hardware

The protections are split up in the following order:

- I2C related protections.
- ADOC related protections (via polling on I/O pins or via algorithms).
- DOP related protections (mainly for deflection items).
- Hardware errors that are not sensed by the OTC (e.g. vertical flyback protection, bridge coil protection, E/W protection, arcing protection).

All faults detected are re-checked five times before the protection mode is triggered. It should be noted that supply

fault detection/protection must be enabled only after the chassis power supply has been established. Likewise, after the line drive starts, the deflection detection/protection must be enabled. To prevent false activation of protection mode during power mode transitions, interrupts related to supply fault and deflection fault are disabled.

### 5.7.2 I2C Related Protections

In normal operation, some registers of the I2C controlled ICs are refreshed every 200 ms. During this sequence, the I2C busses and the I2C ICs are checked.

An I2C protection will take place if the SDA and SCL lines are short-circuited to ground, or to each other. An I2C error will also occur, if the power supply of the IC is missing.

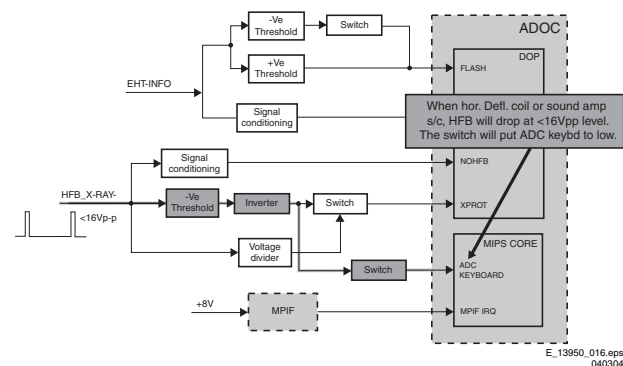
### 5.7.3 ADOC Related Protections

If a protection is detected at an ADOC input, the uP will start to scan all protection inputs every 200 ms for five times. If the protection on one of the inputs is still active after 1 s, the microprocessor will put the set in the protection mode. Before the scanning is started, a so-called "ESD refresh" is carried out. This is done, because the interrupt on one of the inputs is possibly caused either by a flash or by ESD. As a flash or ESD can influence IC settings, the key ICs are initialized again, to ensure the normal picture and sound conditions of the set.

#### Under Voltage Protection

The under voltage protection is needed due to the non-isolated chassis architecture used in A02. Whenever there is a short circuit in the Deflection yoke coil or in the Audio power supply, the averaged Horizontal Flyback Voltage (HFB\_XRAY\_PROT) will fall. After signal conditioning, this voltage is fed to the "KEYBOARD\_ADC" input. When this input of the MIPS controller is less than a certain level, the under voltage protection is activated. This is done by the normal keyboard polling mechanism.

The protection mode is activated after five consecutive occurrences. Response time required is 2 s. This is to avoid set going to under voltage protection mode during start up, since the HFB will only be stable w.r.t. mains on for about 1.6 s.



**Figure 5-2 Under Voltage Protection**

#### +8V Protection

Hardware is employed for the detection of +8V supply fault. A hardware interrupt (MPIF-IRQ) is generated by the MPIF when the +8V supply falls below the IC specification.

To avoid false detection, the corresponding interrupt sub routine checks the status of "ASUP" bit in the MPIF status register for five times consecutively with an interval of 200 ms before triggering the protection mode. Response time required is 1.2 s.



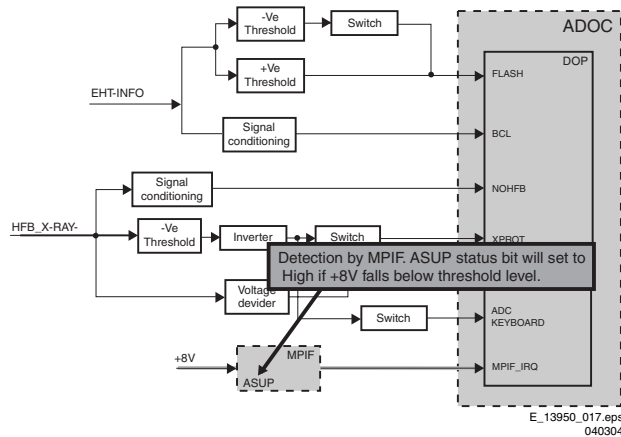


Figure 5-3 +8V Protection

### 5.7.4 DOP Related Protections

The uP reads every 200 ms the status register of the DOP (via the I2C bus). If a protection signal is detected on one of the inputs of the DOP, the relevant error bit in the register is set to "high". If this error bit is still "high" after 1 s, the OTC will store the error code in the error buffer of the NVM and, depending on the relevancy of the error bit, the set will either go into the protection mode or not.

#### Horizontal Fly Back Protection

Hardware is employed for the detection of a horizontal deflection fault. The DOP core generates a hardware interrupt when consecutive three horizontal flyback pulses are not received at the HFB input of the DOP block of the ADOC IC. To avoid false detection, the corresponding interrupt sub routine checks the status of "NOHFB" status bit in the DOP core for five times consecutively with an interval of 50 ms before triggering the protection mode. The response time for this protection needed is 300 ms.

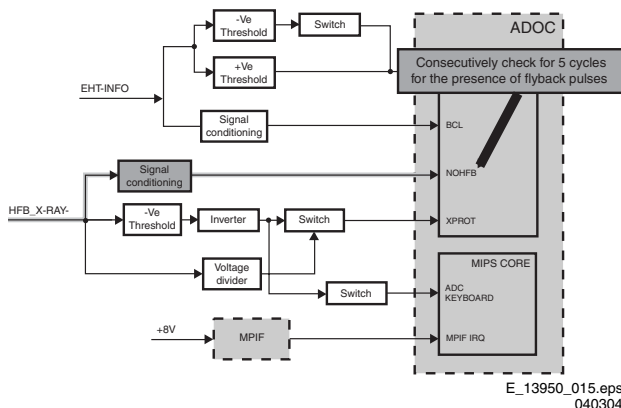


Figure 5-4 Horizontal Fly Back Protection

#### X-Ray Protection (Over Voltage, USA only)

Hardware is employed for the detection of X-ray fault. A hardware interrupt is generated by the DOP core when the "XPROT" input of ADOC IC is pulled "HIGH" (flyback pulses are > 27 V<sub>pp</sub>).

To avoid false detection, the corresponding interrupt sub routine checks the status of "XPROT" bit in DOP core for five times consecutively with an interval of 50 ms before triggering the protection mode. It should be noted that the "XPROT" status is not reset on reading. It should be cleared by the software explicitly.

Once the XRAY protection status is confirmed, the "PRD" bit has to be set to "1" by software. This enables an automatic stop of the H-out via Slow Stop initiated by auto-clearing the DFL bit. Now, the protection mode is activated.

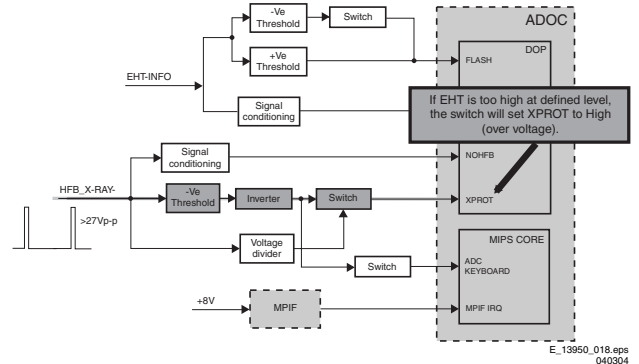


Figure 5-5 X-Ray Protection

#### Beam Current Protection

A hardware interrupt is generated by the DOP core when the current at the BCL input of the ADOC IC exceeds the limit. To avoid false detection, the corresponding interrupt sub routine checks the status of "BCF" bit in DOP core for five times consecutively with an interval of 50 ms before triggering the protection mode. Once the BCL protection status is confirmed, the "PRD" bit has to be set to "1" by software. This enables an automatic stop of the H-out via Slow Stop initiated by auto-clearing the "DFL" bit. Now, the protection mode is activated.

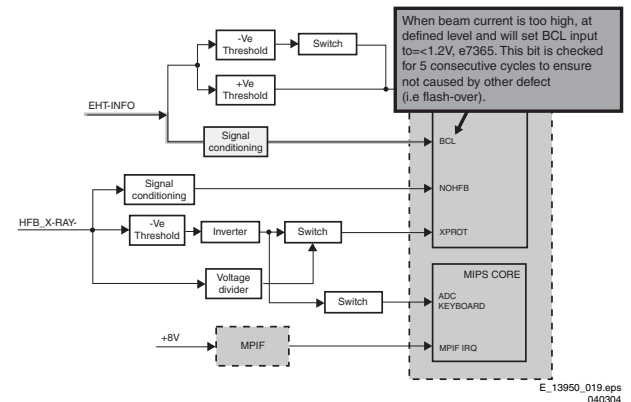


Figure 5-6 Beam Current Protection

#### Flash Protection

Flash detection is used to shutdown the set only if the Flash occurs more than five times and is persistent. Therefore, this is a method to protect the set from undue electrical stress because of picture tube flashes. The flash detector circuitry uses the "EHT\_INFO" signal as input. Its output is connected to the "FLASH" input of the DOP block of the ADOC. When the "FLASH" input is pulled "HIGH", the ADOCs horizontal drive output stops immediately and the "FPR" status bit of the DOP core is set to "1". The status is latched until readout. With the absence of any other disturbances, the horizontal drive output will restart after the "FLASH" input is "LOW" again. No software interaction is required in this case. The "FPR" bit has to be readout by polling at an interval of 500 ms. If the "FPR" status bit has been set to "1" for more than five times consecutively, then the protection mode is triggered. Setting the "FPR" bit for less than five times by the "FLASH" input does not trigger the protection mode (shutting down of the H-drive is enough).

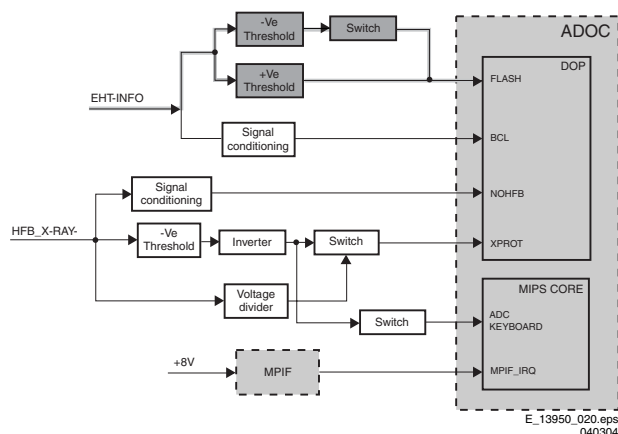


Figure 5-7 Flash Protection

### 5.7.5 Hardware Related Protections

Due to the architecture (read: "hot" deflection), some protections cannot be sensed by the microprocessor. These protections will lead to a protection on set level (Standby mode and blinking LED).

#### Arc Protection

If there are "open" connections (e.g. bad solder joints) in the high-energy deflection circuitry, this can lead to damaging effects (read: fire). For that reason, the E/W current is sensed (via 3479//3480). If this current becomes too high, the "thyristor" circuit (TS7653 and TS7654) is triggered. TS7442 is switched "on" and TS7443 is forced into conduction. The "SUP-ENABLE" signal is shorted now to ground level, which will force the Main Power Supply to Standby mode. This prevents further arcing.

#### Vertical Protection

If the frame stage generates no pulses, TS7641 will block. TS7443 is now switched "on", which will lead to Standby mode. Therefore, in normal operation condition, TS7641 and TS7652 are conducting, while TS7443 is blocked.

#### EW protection

Several faults in the deflection circuit can cause excessive currents through MOSFET 7480. The temperature of this device can become too high, causing an unsafe situation. The power supply is shut down in the above-mentioned way.

**Caution:** All hardware deflection protections can be disabled by interrupting R3403 on the LSP.

**However, be careful:** unsafe situations (heat) can occur or the picture tube can be destroyed.

#### Bridge coil protection

According safety regulations, every coil may be short-circuited. By doing this in the secondary winding of coil L5422, high currents will flow in the winding. With no safety circuit, the coil will begin to burn soon.

This is sensed via the "EW" signal going to the base of TS7652 (via R3495 and D6499). In a normal situation, the voltage on C2498 (diagram A4) is high and TS7652 is conducting. When bridge coil 5422 (diagram A3) is short circuited, the voltage on C2498 changes to low, which will block TS7652. In this case, also TS7641 will block and the voltage on 2642 will rise until TS7443 is forced in conduction. The "SUP-ENABLE" signal (in normal operating condition -20 V) is shorted now to ground level, which will force the Main Power Supply to Standby mode.

**Note:** Maximum EW width settings can also cause a protection.

## 5.8 Repair tips

### 5.8.1 Miscellaneous

The relay you hear when you switch the set "on" (from Standby or via the AC power switch), is from the degaussing circuitry. It is **not** used for switching the Power Supply (as done in the MG-chassis).

- Where the circuitry was too "crowded" for service printing, you can find the correct location on the "test point overviews" in this manual.
- **A very large part of the LSP is "hot"**, such as:
  - The primary part of the Standby Supply.
  - The whole Main supply (except for the secondary Audio supply).
  - And the complete deflection circuitry (so notice that the deflection coil is hot!).

### 5.8.2 Start-up/Shut-down Sequence

For a detailed description, see chapter 9 "Circuit Descriptions, Abbreviation List, and IC Data Sheets".

### 5.8.3 ComPair

This chassis does not have an IR transmitting LED (as in MG-sets). Therefore, a "Service" (ComPair) connector is implemented at the rear side of the set, which is directly accessible. In addition to this, there is also a blinking LED procedure to show the contents of the error buffer.

When you use ComPair, you have the possibility to activate a "stepwise start-up" mode. With this mode, you can initiate the start-up sequence step by step. This also means that in certain steps, some protections are not activated. This is sometimes very convenient during repair.

### 5.8.4 Protections

Activating SDM via the "service pads" will overrule the processor-controlled protections, but **not** the hardware protections.

**Caution:** When doing this, the service technician must know what he is doing, as it could lead to damaging the set.

The "ARC"- and/or "BRIDGECOIL" protection are hardly ever triggered, however:

- When you suspect the "ARC" protection, look for bad solder joints and smell. By interrupting resistor 3497, this protection is disabled (special attention needed!).
- When you suspect the "BRIDGECOIL" protection, which can also be due to a too wide picture amplitude, shorten G and S of the E/W MOSFET 7480. This will disable the protection. You will now have minimal horizontal amplitude. Re-align the horizontal amplitude in the SAM menu and remove the G/S short of TS7480.



### 5.8.5 Main Supply

1. Replace FET 7504 and zener 6505.
2. Disconnect the SSP panel.
3. Short B and E of TS7529, in order to put the Main Supply in "on"-mode (TS7529 is blocking then).  
**Caution:** To prevent that R3403 and TS7443 will be damaged, **first disable the HW-protection of the deflection circuit.** Therefore, short-circuit C2642 on the LSP (diagram A4).
4. Attach a load of 500 ohm to the V\_BAT capacitor C2515 (the supply can not work without a minimum load).
5. Use a variac, and slowly increase the V\_MAINS. Measure over sensing resistors R3514//15, if a nice sawtooth voltage becomes available.
6. Also, measure the V\_BAT. This may never exceed +141 V. If it does, there is something wrong in the feedback circuitry (e.g. regulator 7506).

**Note:** Be careful when measuring on the gate of FET TS7504. This circuitry is very high ohmic and can easily be damaged

(first connect ground to measuring equipment, than measure the gate).

### 5.8.6 Frame Deflection

**Caution:** When the Frame Deflection circuitry is suspected, one must be careful. Because there is a DC-voltage on the frame deflection, **the beam current could damage the CRT neck, leading to a defective CRT.**

To prevent this from happening, you must:

1. Interrupt the resistors 3403 and 3404 on the CRT panel (diagram F), in order to remove the "filament" voltage from the tube (no beam current, so no chance of destroying the CRT).
2. Interrupt resistor 3403 on the LSP (diagram A4) to disable the "SUP-ENABLE" line.
3. Measure with a multi-meter, or better with an oscilloscope, the functionality of the Frame stage.
4. After you have found the cause, exchange the defective component (e.g. TDA8177), and re-solder the interrupted resistors.

**Table 5-3 Repair tips**

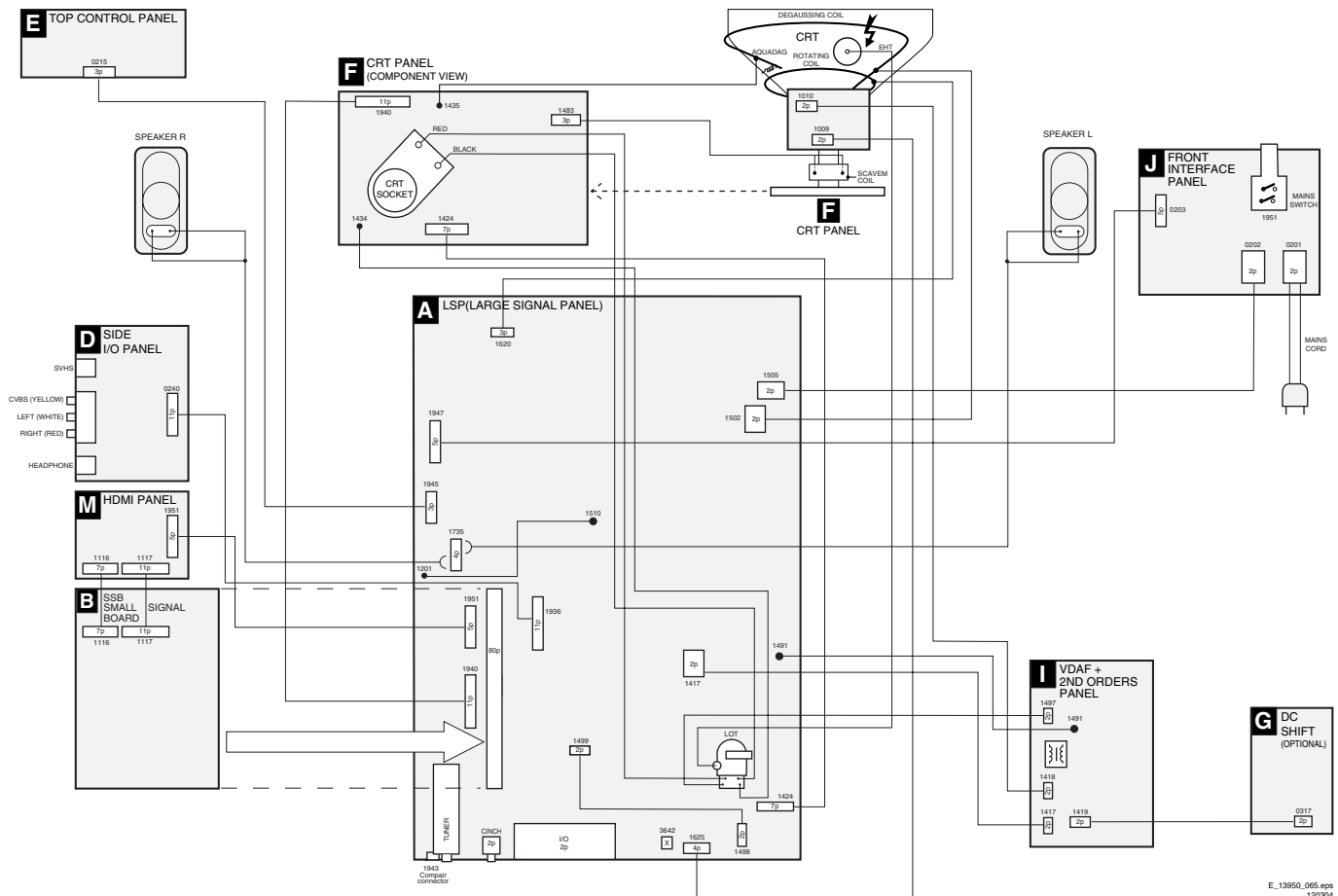
Phenomenon	Possible Cause	Repair tip
No picture, no LED.	Standby Supply defective.	Measure circuitry (see diagram A2). Start at test-point A19. When the Mains switch is "on", this voltage must always be available.
No picture, LED blinking at 3 Hz.	Set is in protection due to various causes. For error codes see error-code list.	You have no picture, so: read the error buffer via ComPair (error buffer is accessible when set is in protection, ComPair-file will guide you to this). Read the blinking LED information via standard remote command mute-06250x-ok. Or you read the error code sequence via standard remote command mute-062500-ok. When you have found the error, check the circuitry related to the supply voltage and I2C-communication or the circuitry that triggers the protection.
No picture, LED blinking with code 8-8-8-etc or 9-9-9-etc.	No communication on slow I2C- or fast I2C-bus.	As processor cannot communicate with one of the 2 busses it the standby-LED spontaneously starts blinking 8-8-8-etc or 9-9-9-etc.... If in the error buffer somewhere is an error 8 or 9, these will have the highest priority starting the mentioned blinking. Measure dependent of the error on the I2C-bus which device is loading the bus (use the I2C-overview)
No picture, LED blinking with code 13-13-13-etc.	No communication on NVM-I2C bus to the uP.	As the uP cannot communicate with the NVM I2C bus, it spontaneously starts blinking 13-13-13-etc. Note: when there is no access to the NVM, a lot of picture setting can go wrong.
No picture, no sound. Set is making audible squeaking sound	Supply is possibly in hiccup-mode, which is audible via a squeaking supply transformer.	Possible causes: V_BAT is shorted (caused by short circuited line transistor 7421), the sound winding is shorted (amplifier is shorting the power supply lines), or D6514 is shorted (due to a too high V_BAT). Remove excessive load, to see what causes the failure, or check feedback circuit. See repair tip "Main Power Supply" (supply needs a minimal load).
No picture, no sound. Front LED works fine	Supply does not work correctly.	If e.g. V_BAT is only about 90 V, it is possible that the regulator IC (7506) is defective.
No RC-reception. Front LED does not echo RC-commands.	uP circuitry or RC-receiver is defective.	In case the set does react on a local keyboard operation, you must check the RC-receiver circuitry (diagram J).
Relay (degaussing) is not audible, when set is switched from "off" or "standby" to "on".	uP is not working correctly. When line "DEGAUS" is low, the degaussing must be activated.	Check RESET-circuitry (IC7581 on diagram B11). Check the level on line "DEGAUS" when you switch the set "on". Signal must be low initially and go to high after approx. 12 s.
Picture is rotated.	Rotation circuitry (if present) on diagram A5, or related supply to it, malfunctions.	Measure test points on diagram A5.
Picture is continuously switching "off" and "on", showing heavy "switch" spots (set does not go into protection).	200 V is missing on CRT panel.	Probably a bad connection from LSP connector 1424 to CRT connector 1424 (diagram F), or an interruption of the 200 V supplies line (e.g. R3341 on circuit F1 is interrupted).
Picture is not sharp.	Focus is possibly mis-aligned or SCAVEM-circuitry does not work correctly.	Re-align the "FOCUS" potmeter on the Line Output Transformer, or check the SCAVEM circuitry on the CRT-panel (diagram F). It is also possible that the DAF circuitry is defective (see diagram I). Check the V_dc values.
Picture is distorted.	Check video-path in Service Default Mode.	Investigate whether there is an error code present in the error buffer. In case there is one, check the I2C-bus and/or supply lines (see overview supply lines). Measure and check signal path Tuner-MPIF-ADOC-RGB amplifier. In case it is a geometry issue, check on diagram A4 opto-coupler 7482, OpAmps 7440/7450 and the Frame circuitry alignments or a possible corrupted NVM (IC7525 on diagram B11).
No menu, no OSD.	Probably a defective uP (ADOC).	
No Teletext.	IC7730 defective or not powered.	Check circuitry around IC7730 on diagram B13.
Strange switch "off" behaviour	TS7445 possibly defective.	Check, with a multi-meter, whether transistor TS7445 is well functioning. (diagram A3).
Various symptoms, due to missing local supply voltage.	An interrupted fuse, NFR-resistor or connection.	When no symptom or error code leads you to a specific circuitry, use the supply lines overview (see supply lines overview), for a quick scan of all supply lines.

## 5.9 Software Downloading

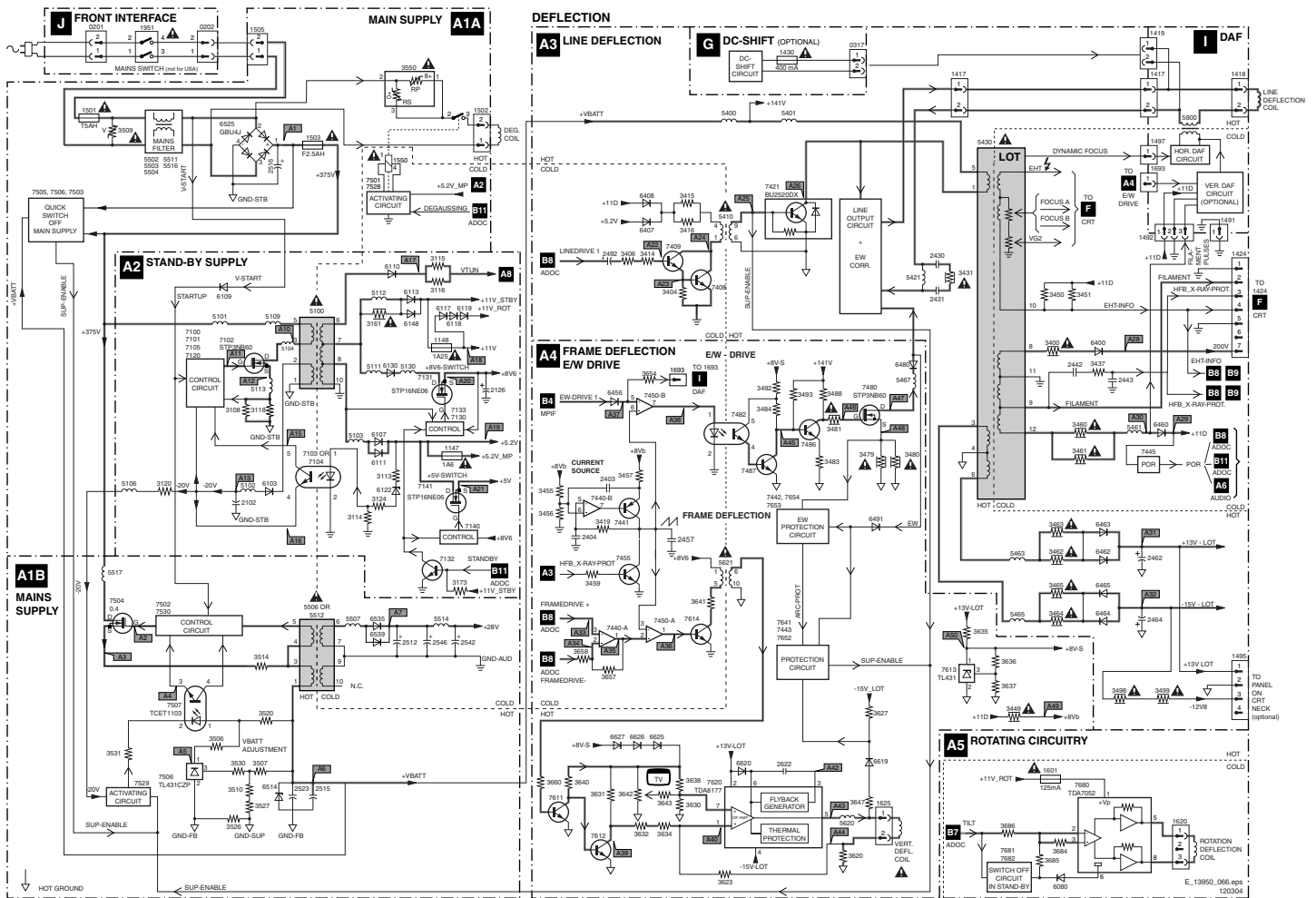
In this chassis, you can **upgrade** the software via ComPair. You can find more information on how this procedure works in the ComPair file. It is possible that not all sets are equipped with the hardware, needed to make software upgrading possible. To speed up the programming process the firmware of the ComPair interface can be upgraded. See paragraph "How To Order" for the order number

## 6. Block Diagrams, Testpoint Overview, and Waveforms

### Wiring Diagram

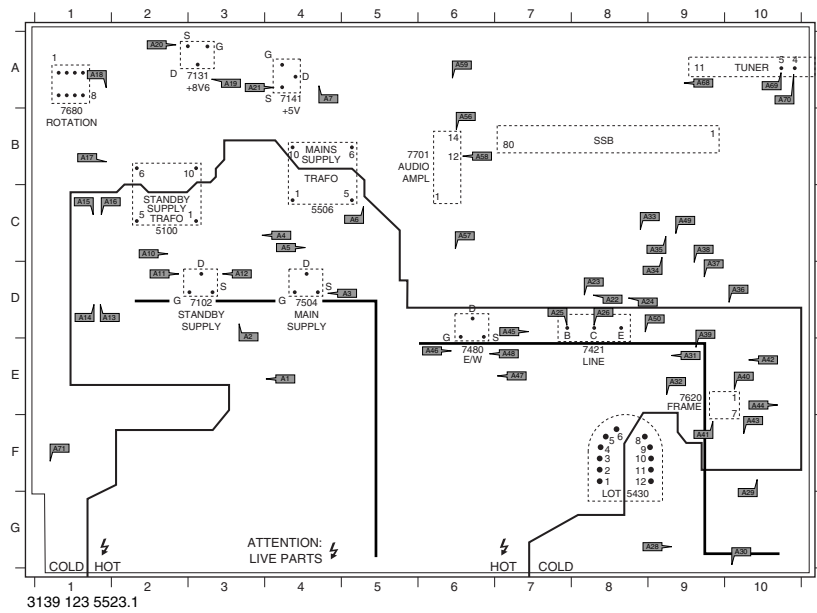
E\_13950\_065.eps  
120304

## Block Diagram LSP Supply and Deflection



## Testpoint Overview LSP and CRT

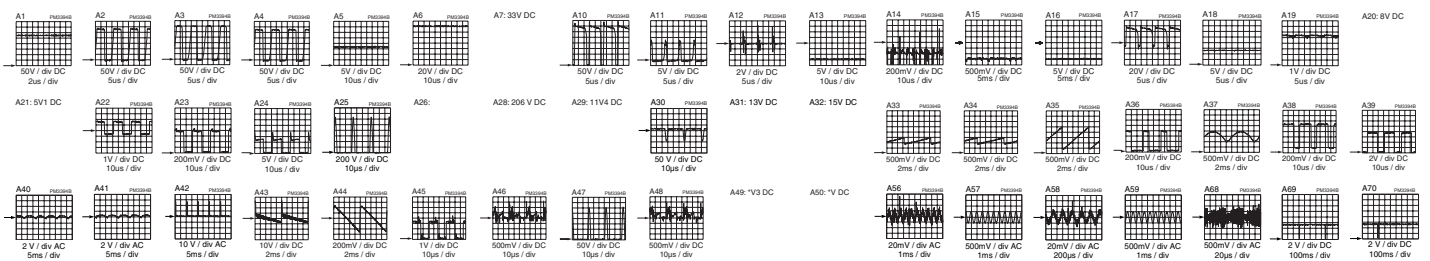
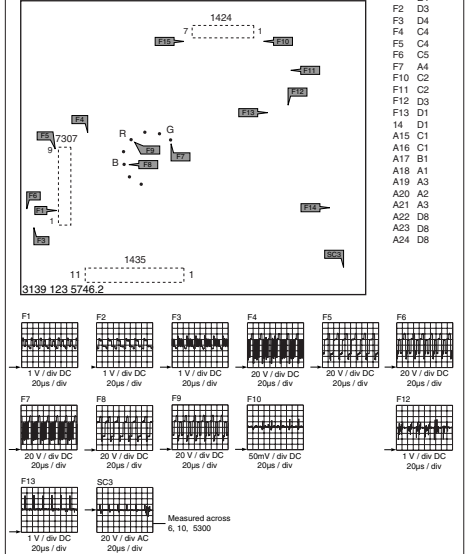
## LSP COPPER TRACK SIDE



A1 E4  
A2 D3  
A3 D4  
A4 C4  
A5 C4  
A6 C5  
A7 A4  
A10 C2  
A11 C2  
A12 D3  
A13 D1  
A14 D1  
A15 C1  
A16 C1  
A17 B1  
A18 A1  
A19 A3  
A20 A2  
A21 A3  
A22 D8  
A23 D8  
A24 D8  
A25 D8  
A26 D7  
A28 G9  
A29 G10  
A30 G10  
A31 E9  
A32 E9  
A33 C8  
A34 D9  
A35 C9  
A36 D10  
A37 D9  
A38 C9  
A39 D10  
A40 E10  
A41 E10  
A42 E10  
A43 F10  
A44 E10  
A45 D7  
A46 E8  
A47 E7  
A48 E7  
A49 C9  
A50 D9  
A56 C6  
A57 B6

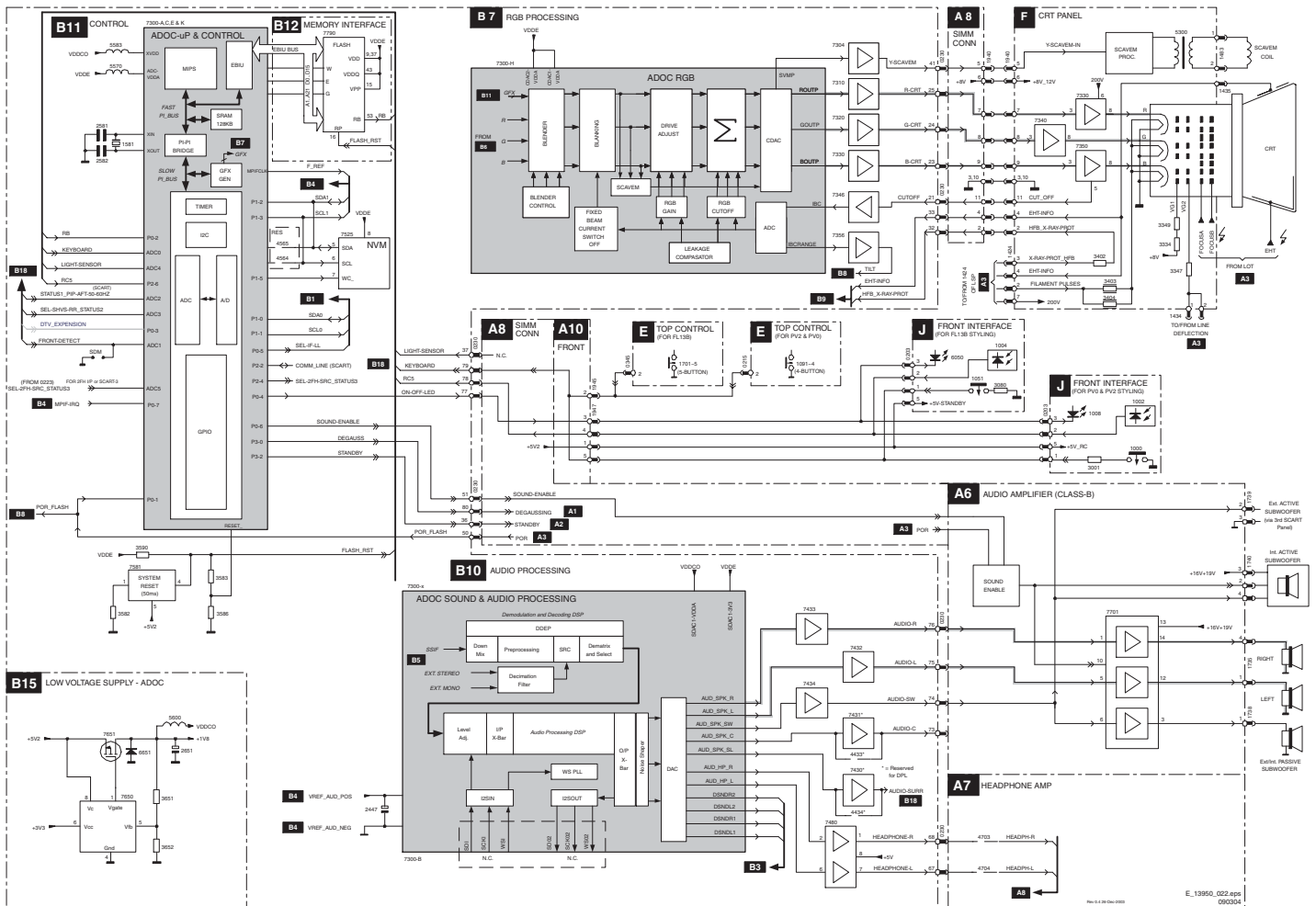
A58 C6  
A59 B5  
A68 A9  
A69 A10  
A70 A10

## CRT PANEL (COPPER TRACK SIDE)



E\_13950\_021.eps  
110304

Block Diagram 2 Audio &amp; Video (A02 NAFTA Video Audio class-B Output)

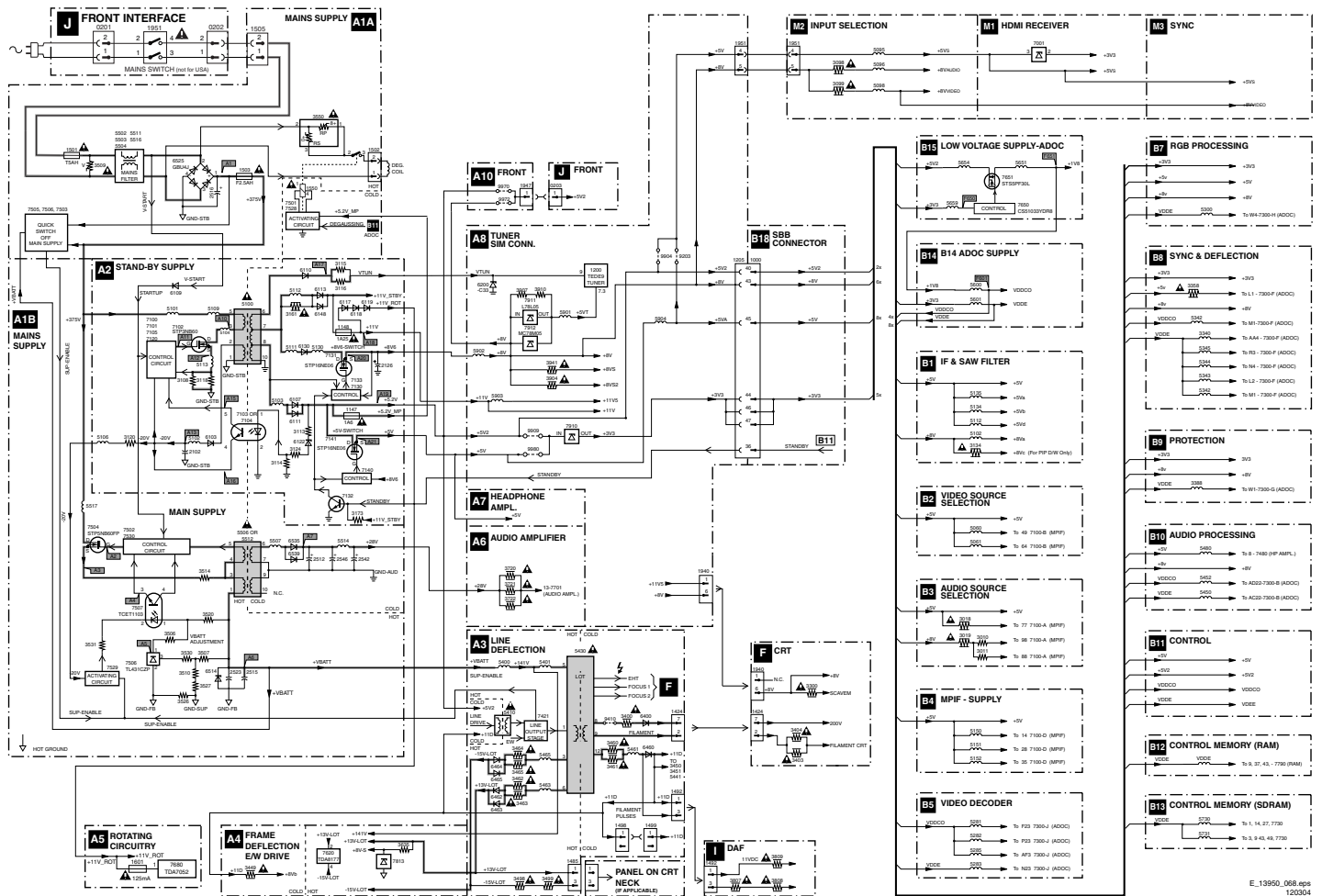








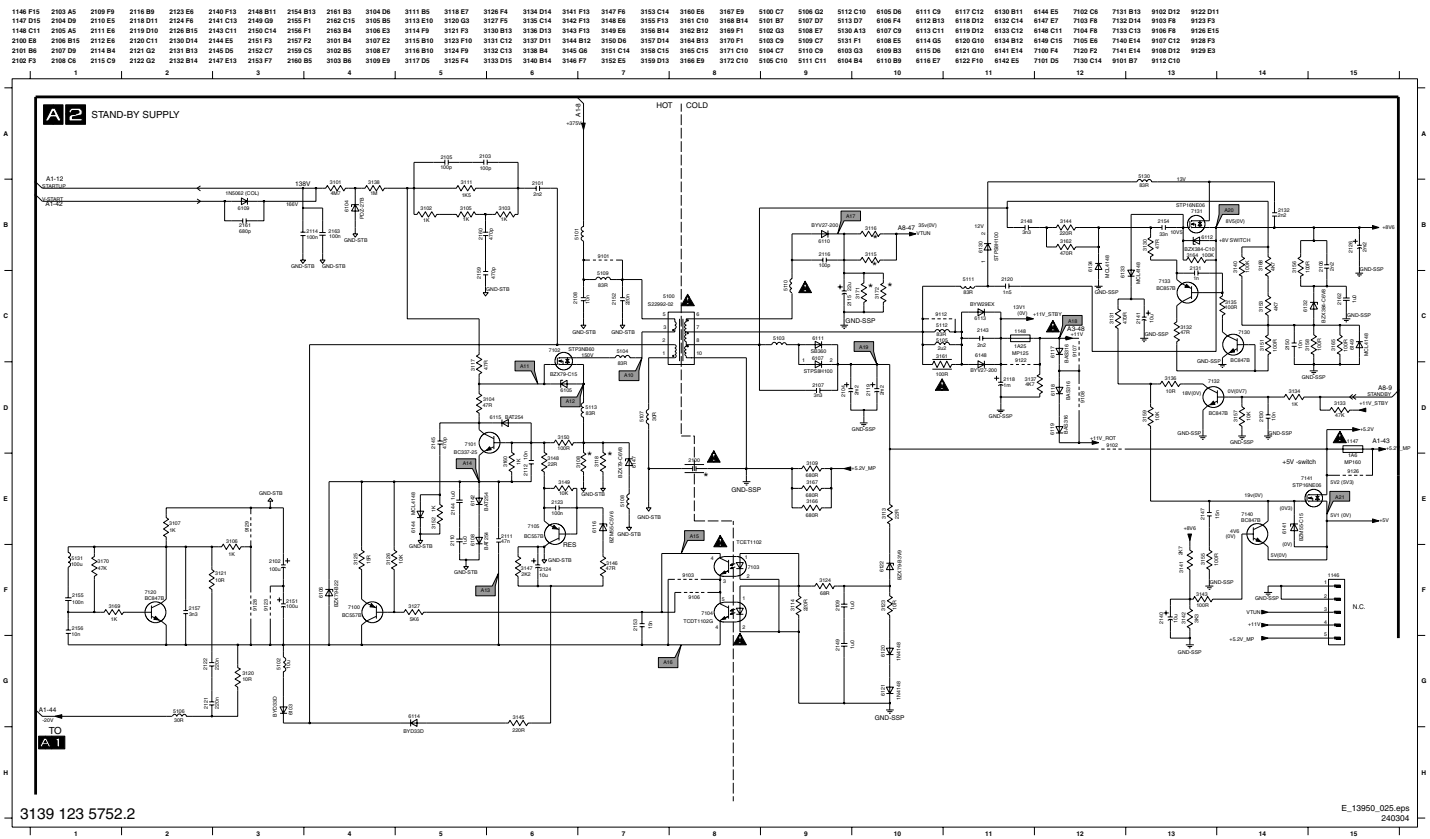
## Supply Lines Overview

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120304

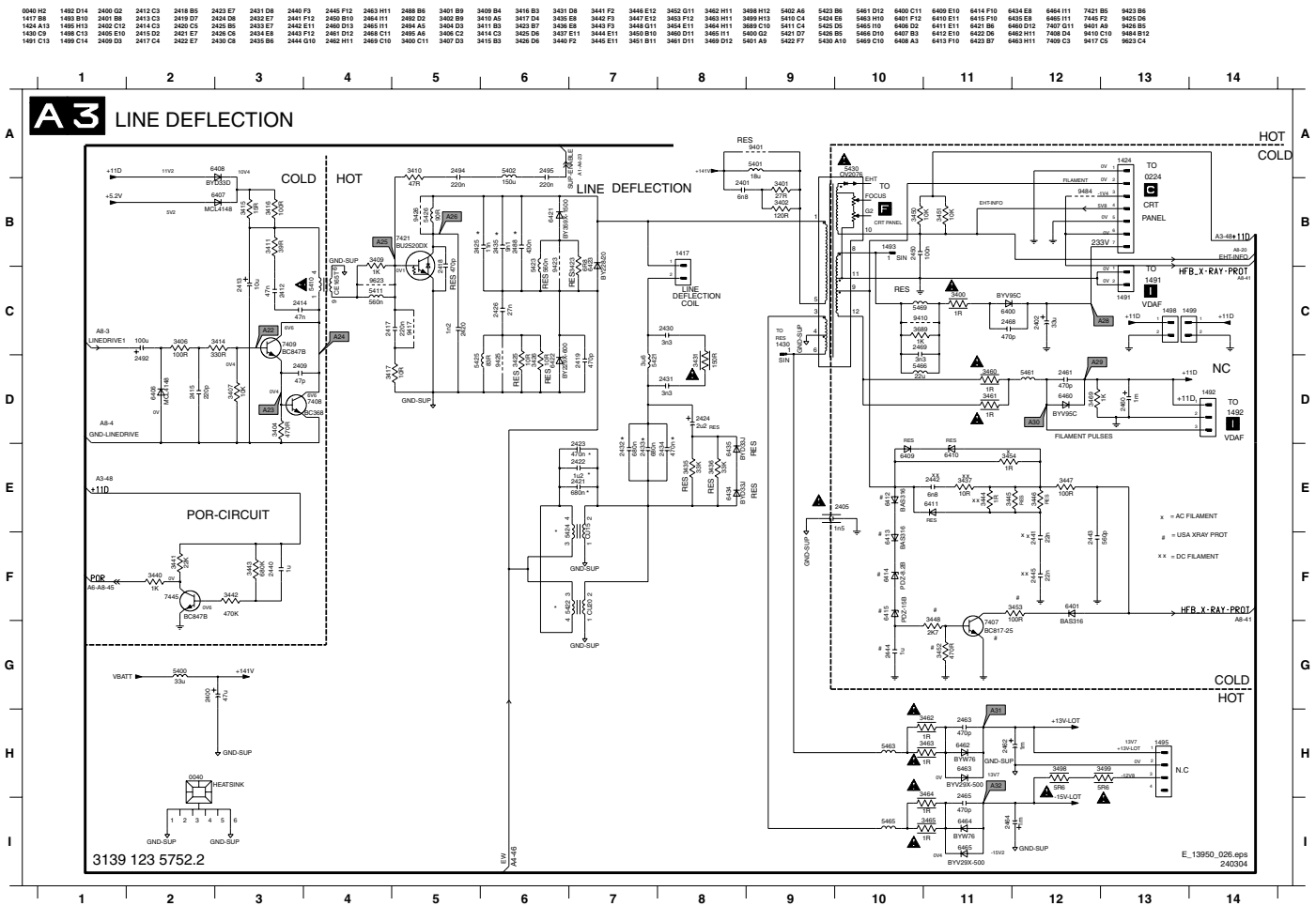




## Large Signal Panel: Standby Supply

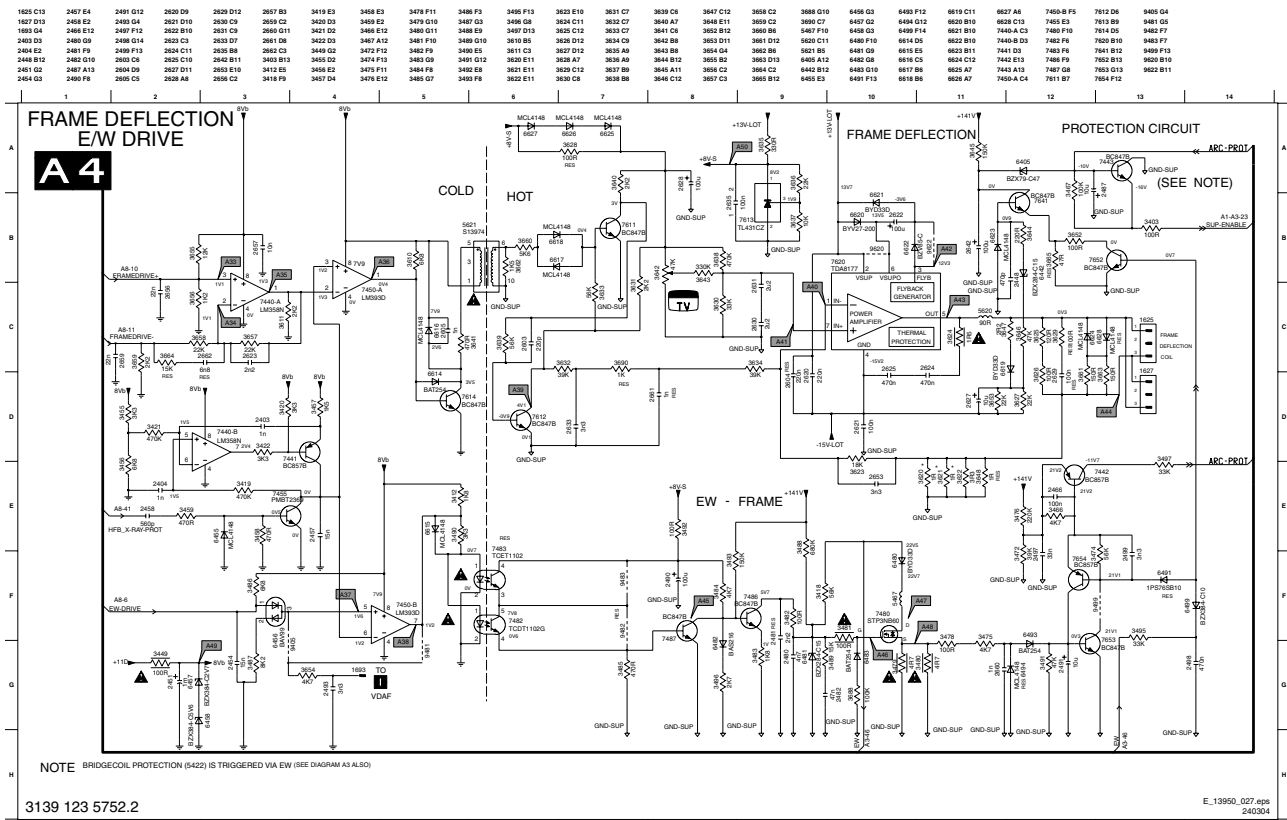


## Large Signal Panel: Line Deflection





## Large Signal Panel: Frame Deflection &amp; E/W Drive

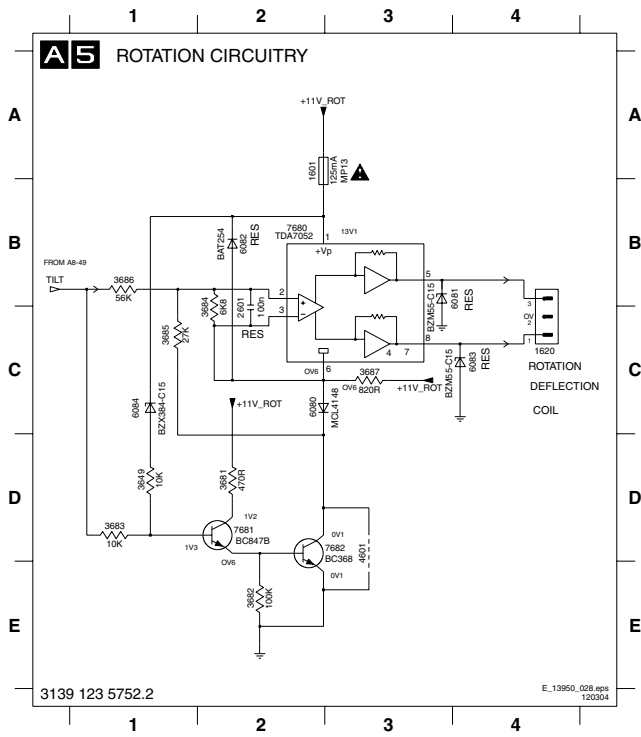


3139 123 5752.2

E\_13950\_027.apx 240304

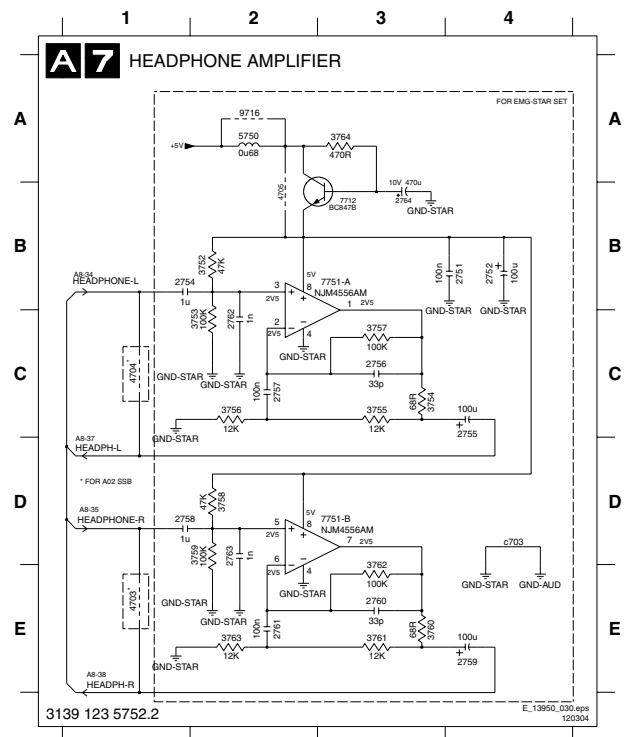
## Large Signal Panel: Rotation Circuitry

1601 A2 2601 C2 3681 D2 3683 D1 3685 C1 3687 C3 6080 C2 6082 B2 6084 C1 7681 D2  
 1620 C4 3649 D1 3682 E2 3684 C2 3686 B1 4601 D3 6081 B3 6083 C4 7680 B2 7682 D3

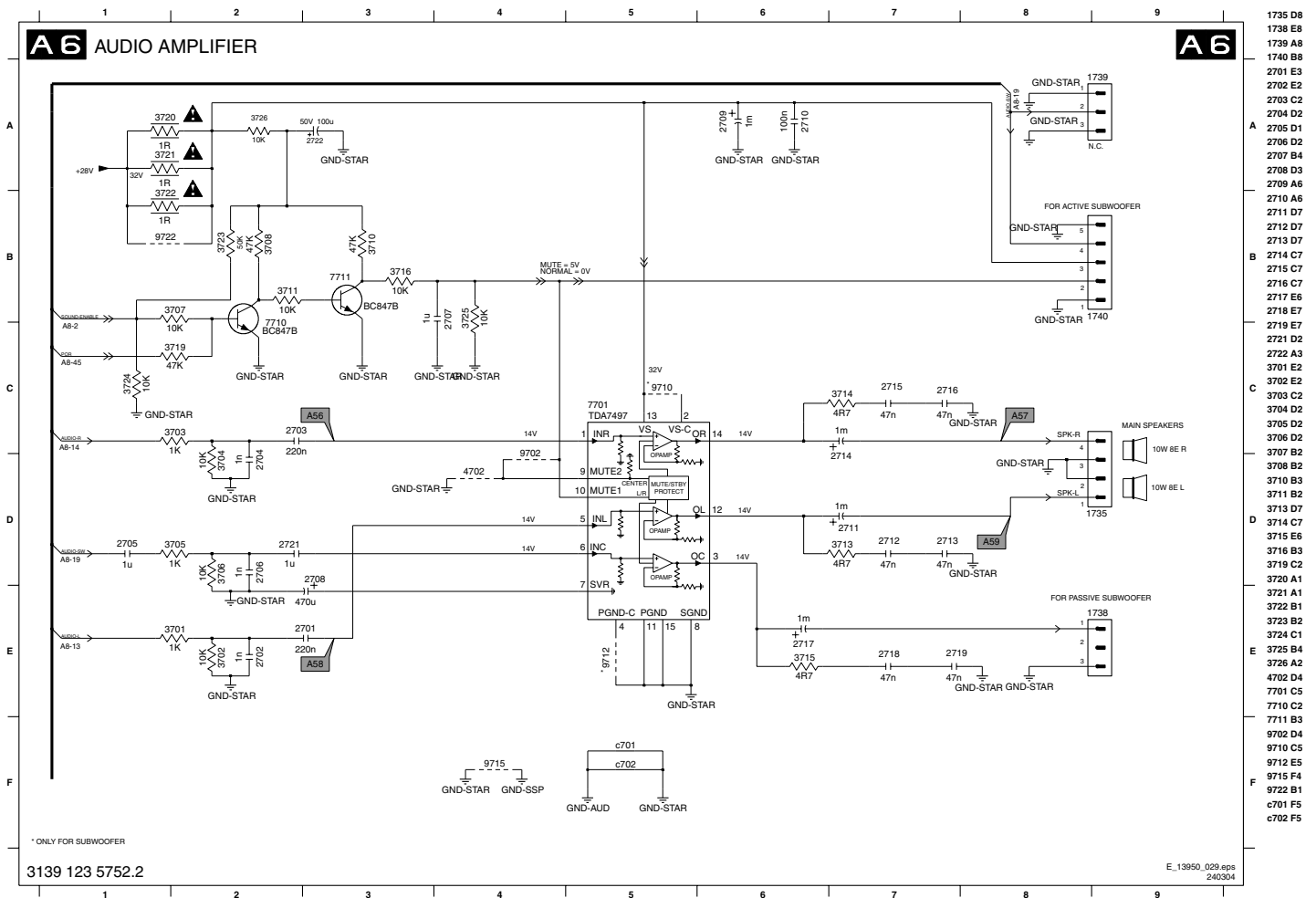


## Large Signal Panel: Headphone Amplifier

2751 B4 2756 C3 2760 E3 2764 B3 3755 C3 3759 D2 3763 E2 4705 B2 7751-B D3  
 2752 B4 2757 C2 2761 E2 2762 B2 3752 C2 3756 E3 3764 A3 5750 A2 9716 A2  
 2754 B1 2758 D1 2762 C2 3753 C2 3757 C3 3761 E3 4703 E1 7712 B3 c703 D4  
 2755 C4 2759 E4 2763 D2 3754 C3 3758 D2 3762 E3 4704 C1 7751-A B3

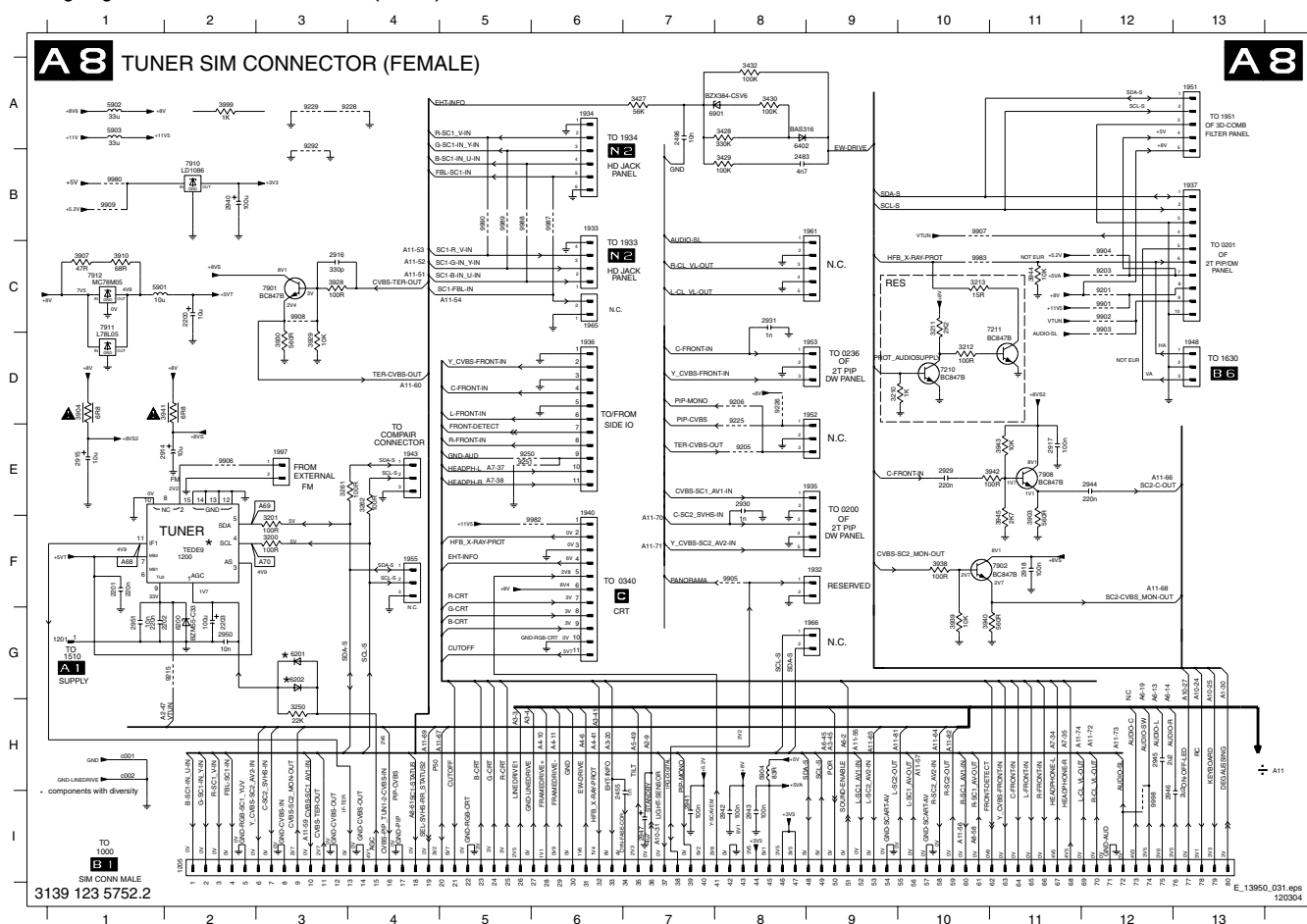


## Large Signal Panel: Audio Amplifier



1735 D8  
1738 E8  
1739 A8  
1740 B8  
2701 E3  
2702 E2  
2703 C2  
2704 D2  
2705 D1  
2706 D2  
2707 B4  
2708 D3  
2709 A6  
2710 A6  
2711 D7  
2712 D7  
2713 D7  
2714 C7  
2715 C7  
2716 C7  
2717 E5  
2718 E7  
2719 E7  
2721 D2  
2722 A3  
3701 E2  
3702 E2  
3703 C2  
3704 D2  
3705 D2  
3706 D2  
3707 B2  
3708 B2  
3710 B3  
3711 B2  
3713 D7  
3714 C7  
3715 E6  
3716 B3  
3719 C2  
3720 A1  
3721 A1  
3722 B1  
3723 B2  
3724 C1  
3725 B4  
3726 A2  
4702 D4  
7701 C5  
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9702 D4  
9710 C5  
9712 E5  
9715 F4  
9722 B1  
c701 F5  
c702 F5

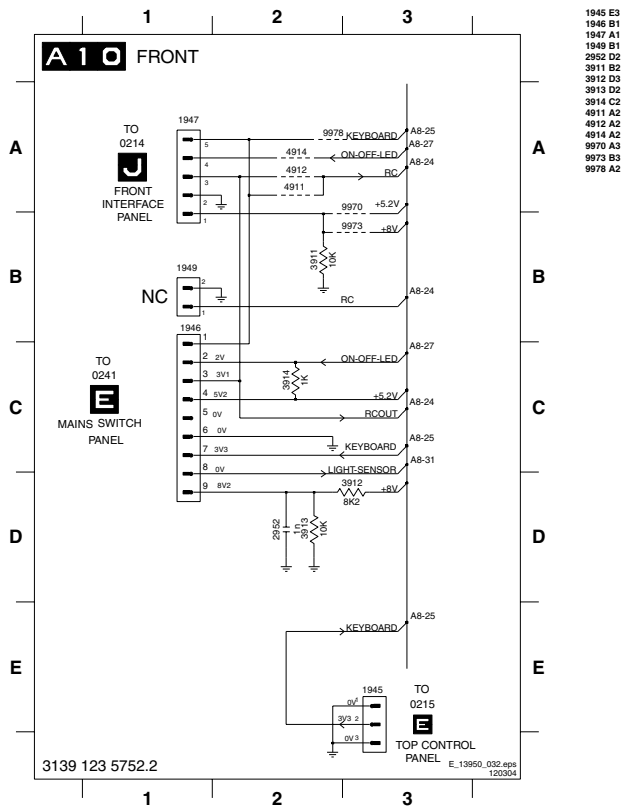
**A8** TUNER SIM CONNECTOR (FEMALE)



1200 F2	9980 B1
1201 G1	9982 F6
1205 I2	9983 C1
1932 F9	9987 B6
1933 B6	9988 B5
1934 A6	9989 B5
1935 E8	9990 B5
1936 D6	9998 I2
1937 B13	c001 H1
1940 F6	c002 H1

1943 E  
1951 A  
1951 A13  
1952 F  
1953 D  
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## Large Signal Panel: Front

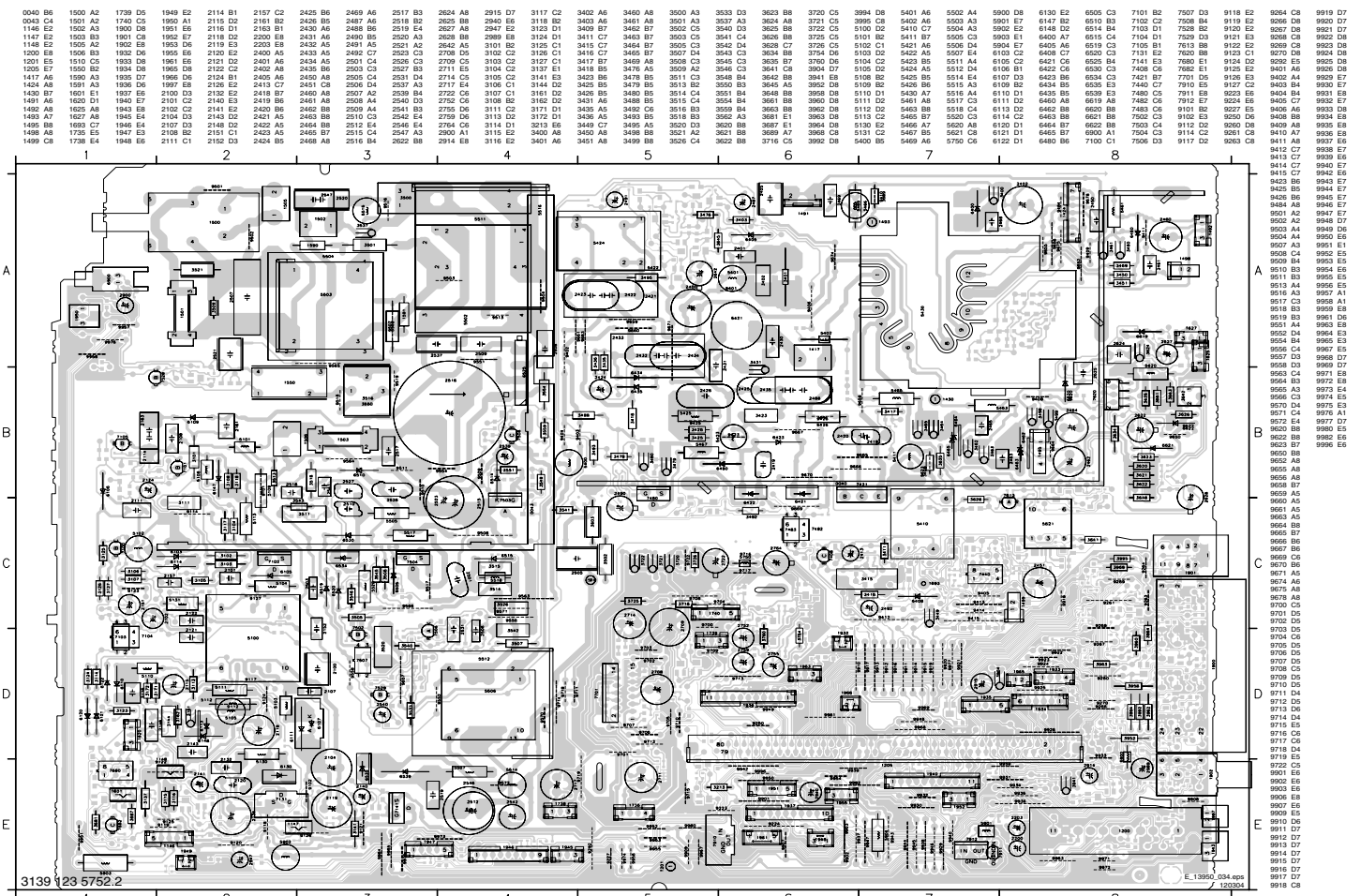


## Personal Notes:

1945 E3
1946 B1
1947 A1
1948 B1
2952 D2
3911 B2
3912 D3
3913 D2
3914 C2
4911 A2
4912 A2
4914 A2
9970 A3
9973 B3
9978 A2

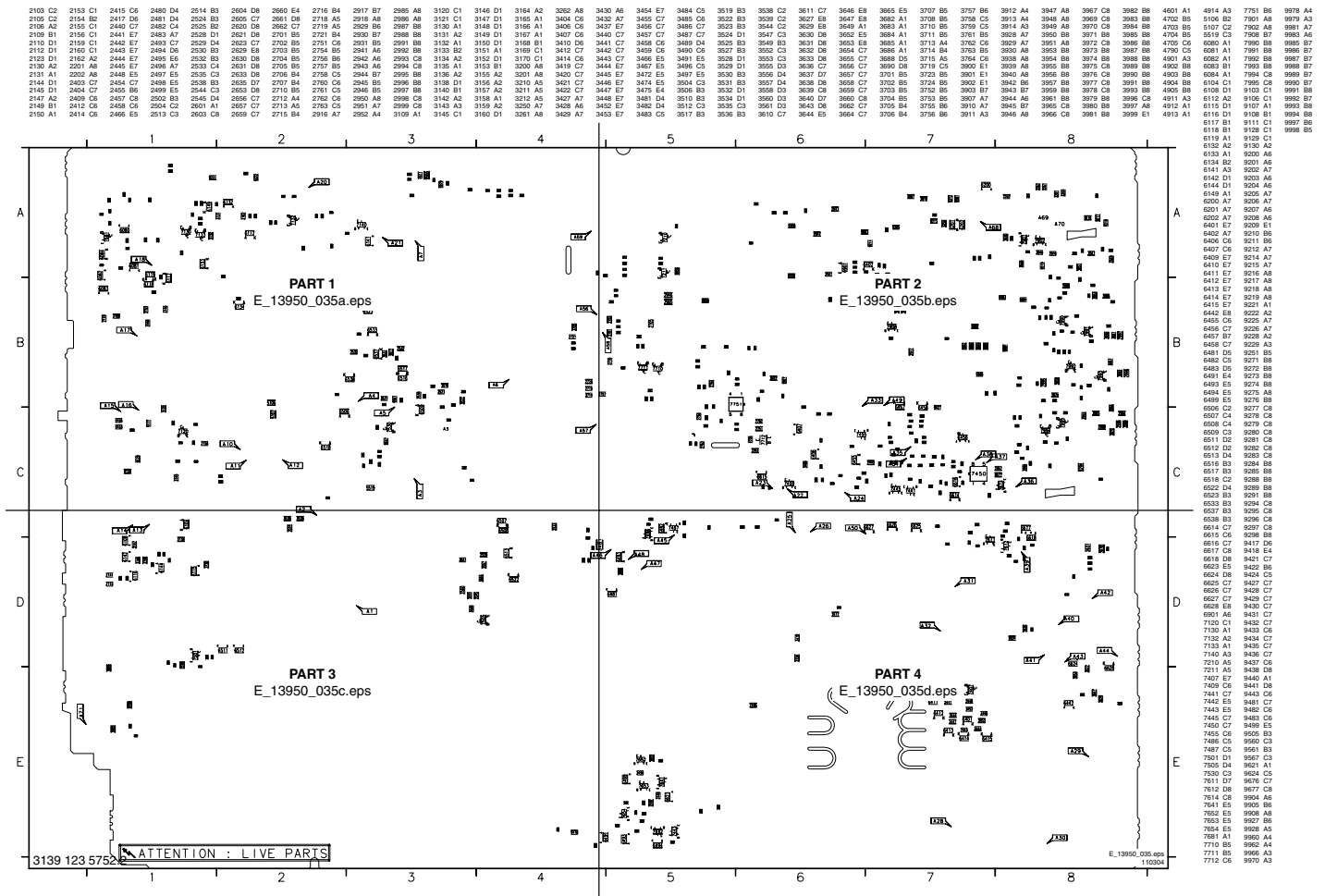


## Layout LSP (Top Side)



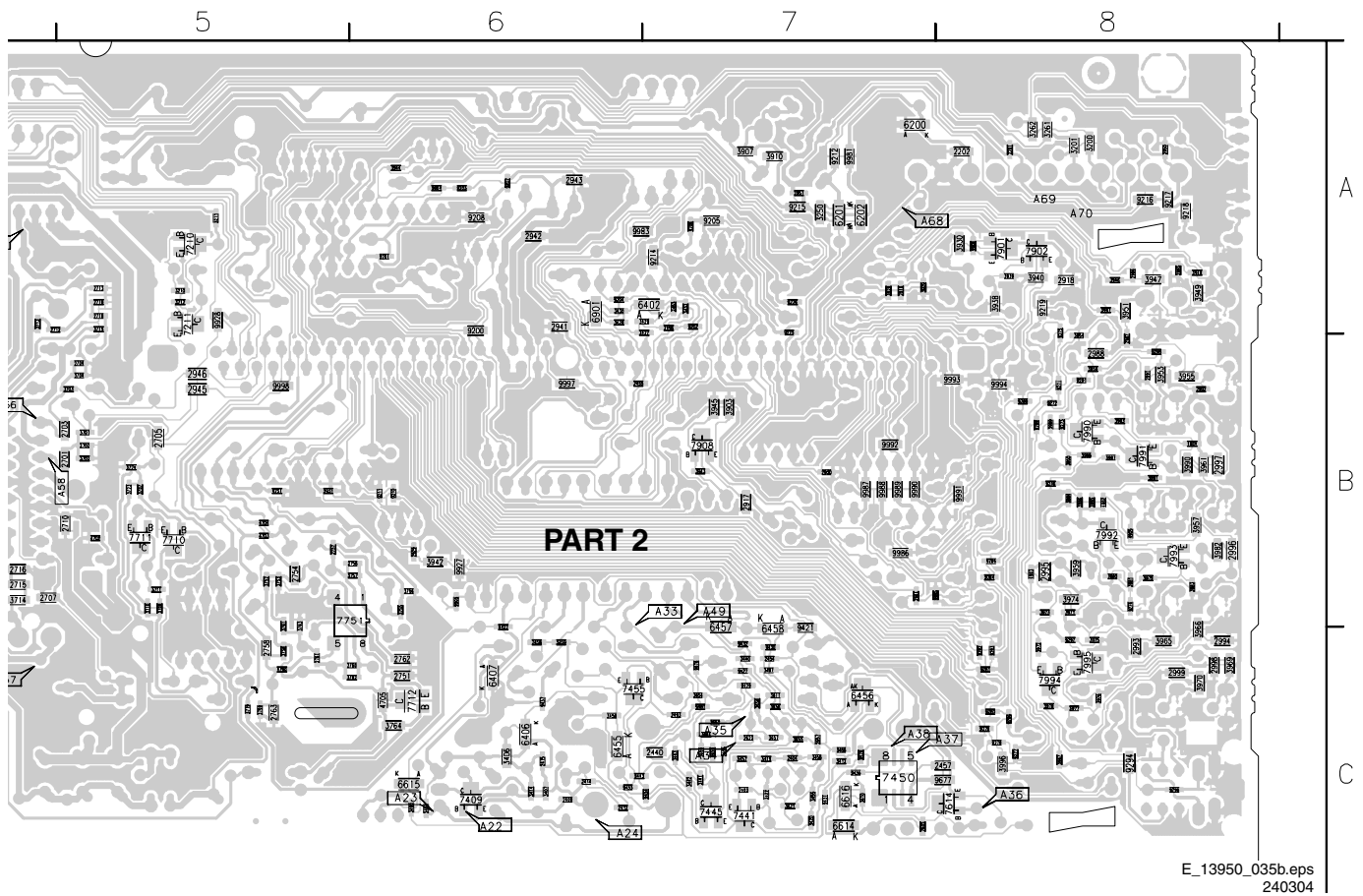


## Layout LSP (Overview Bottom Side)

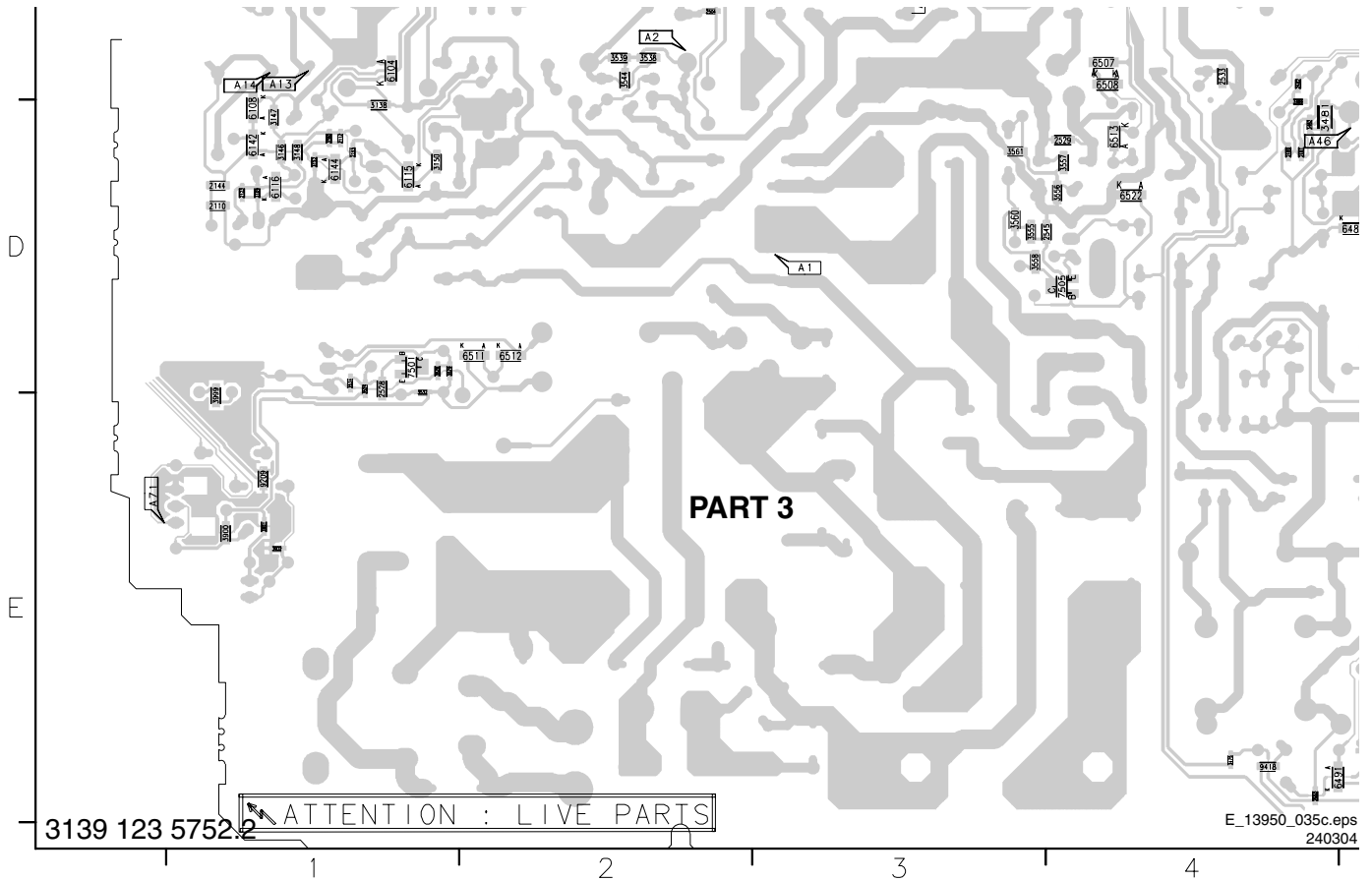


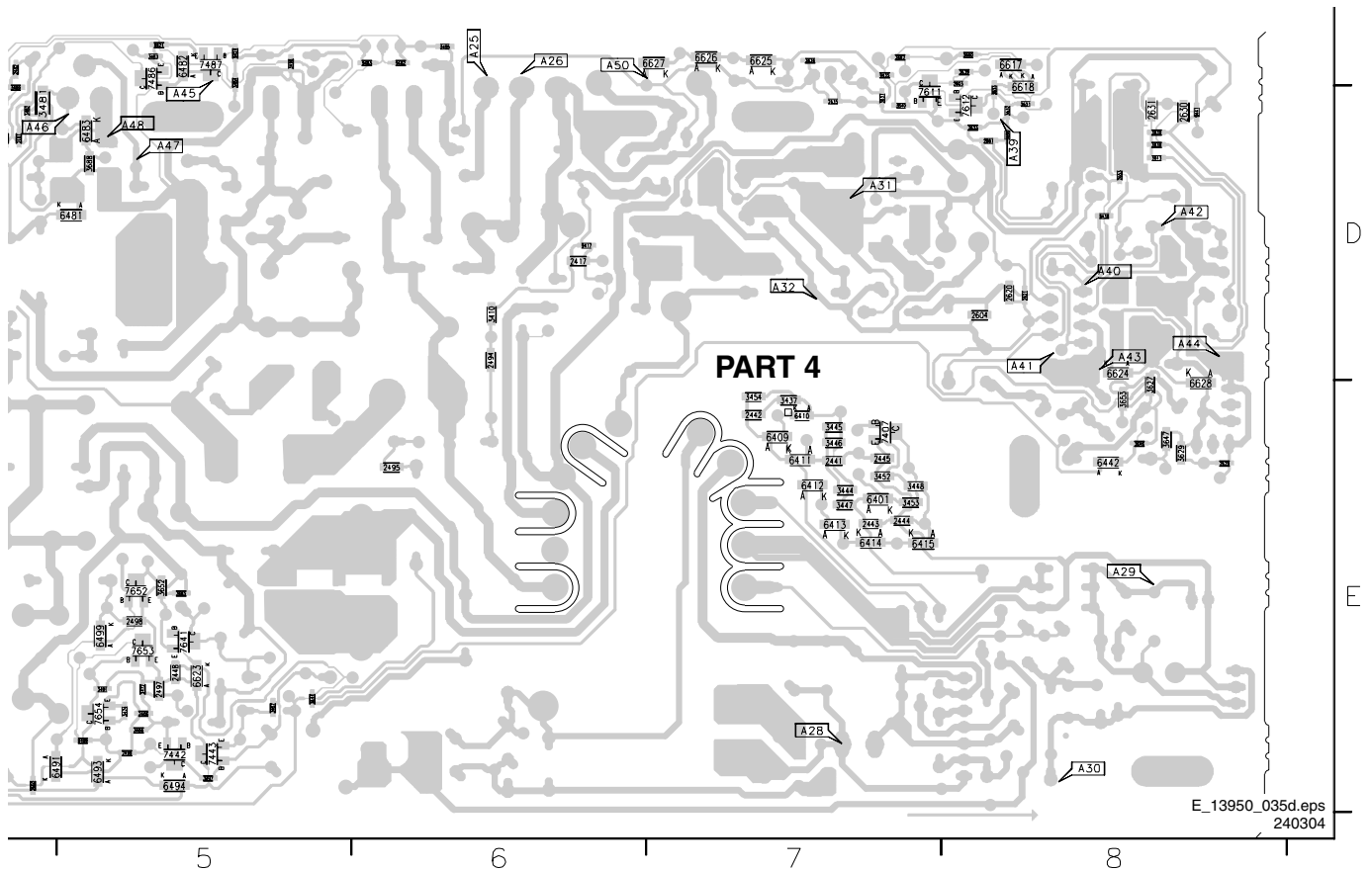


## Layout LSP (Part 2 Bottom Side)



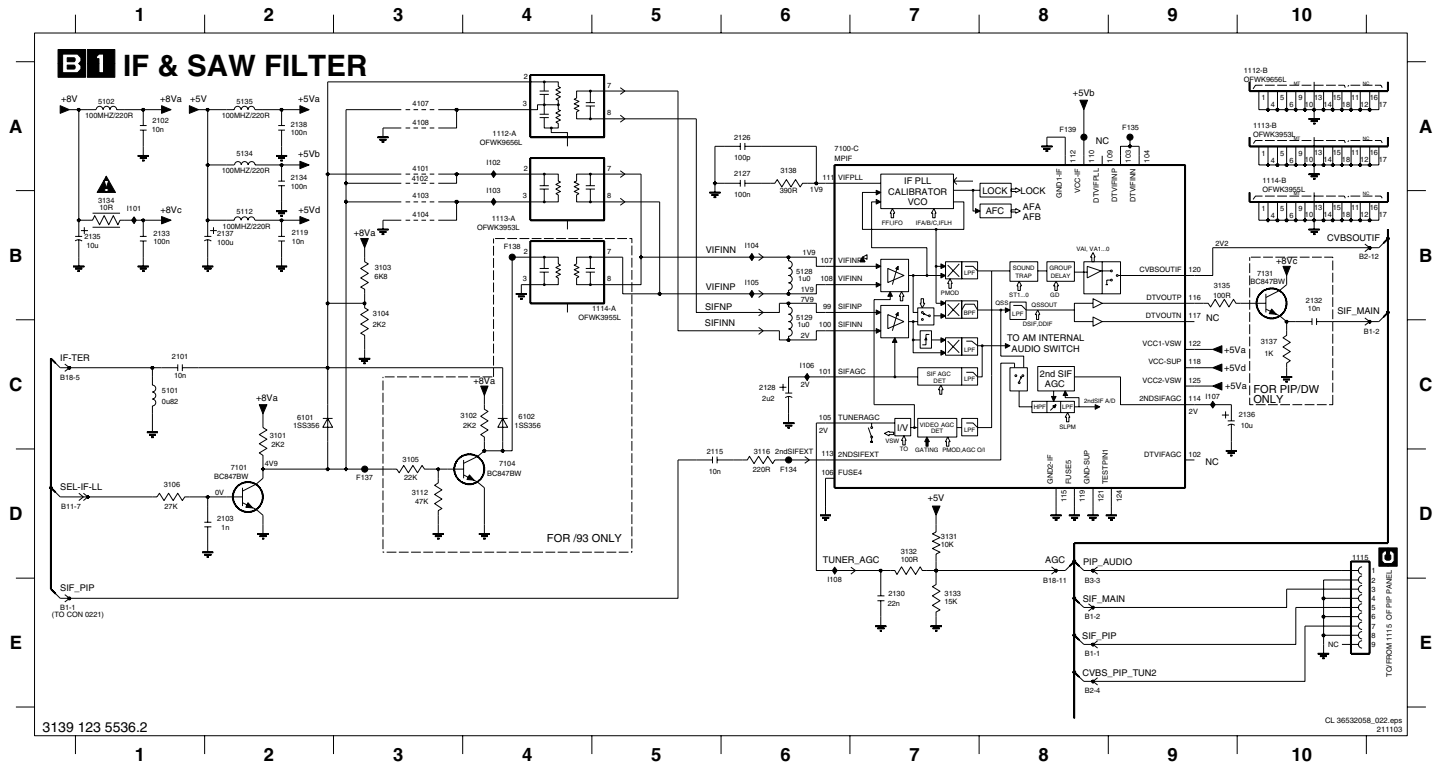
## Layout LSP (Part 3 Bottom Side)





## Small Signal Board: IF &amp; SAW Filter

1112-A A4	1114-A B5	2102 A1	2126 A6	2132 B10	2136 C10	3102 C4	3106 D1	3132 D7	3137 C10	4103 B3	5101 C1	5129 B6	6102 C4	7131 B10	F132 E10	F138 B4	I103 A4	I107 C9
1112-B A10	1114-B A10	2103 D2	2127 A6	2133 B1	2137 B2	3103 B3	3112 D3	3133 E7	3138 A6	4104 B3	5102 A1	5134 A2	7100-C A6	F114 E10	F134 D6	F139 A8	I104 B6	I108 E6
1113-A B4	1115 D10	2115 D5	2128 C6	2134 A2	2138 A2	3104 B3	3116 D6	3134 B1	4101 A3	4107 A3	5112 B2	5135 A2	7101 D2	F115 D10	F135 A9	I101 B1	I105 B6	
1113-B A10	2101 C1	2119 B2	2130 E7	2135 B1	3101 C2	3105 D3	3131 D7	3135 B9	4108 A3		5128 B6	6101 C2	7104 D4	F116 E10	F137 D3	I102 A4	I106 C6	



1116 E1	2064 C2	2068 D2	2072 E2	2076 E2	2082 A7	2086 D4	3061 A8	3065 C2	3070 B1	3074 E3	5060 E3	7060-B B2	F060 B1	F076 E1	F088 F7	I063 D3
2064 A3	2064 C2	2068 D2	2072 E2	2076 E2	2083 C4	2087 C2	3062 B3	3066 A8	3071 B3	4062 E2	5061 F3	7062 B6	F060 B7	F077 F1	F089 F7	I064 D3
2062 A8	2066 D2	2070 D2	2074 D2	2078 D2	2084 C4	2086 A8	3063 B3	3067 B7	3072 E3	4152 D1	5063 A8	7063 B7	F075 E2	F078 E1	F081 E1	I061 C3
2063 C2	2066 D2	2071 D2	2075 E2	2081 F3	2085 D3	2086 A2	3064 C2	3068 B7	3073 E3	4153 E2	7060-A B3	7100-B B4	F074 F1	F080 B4	I062 C3	

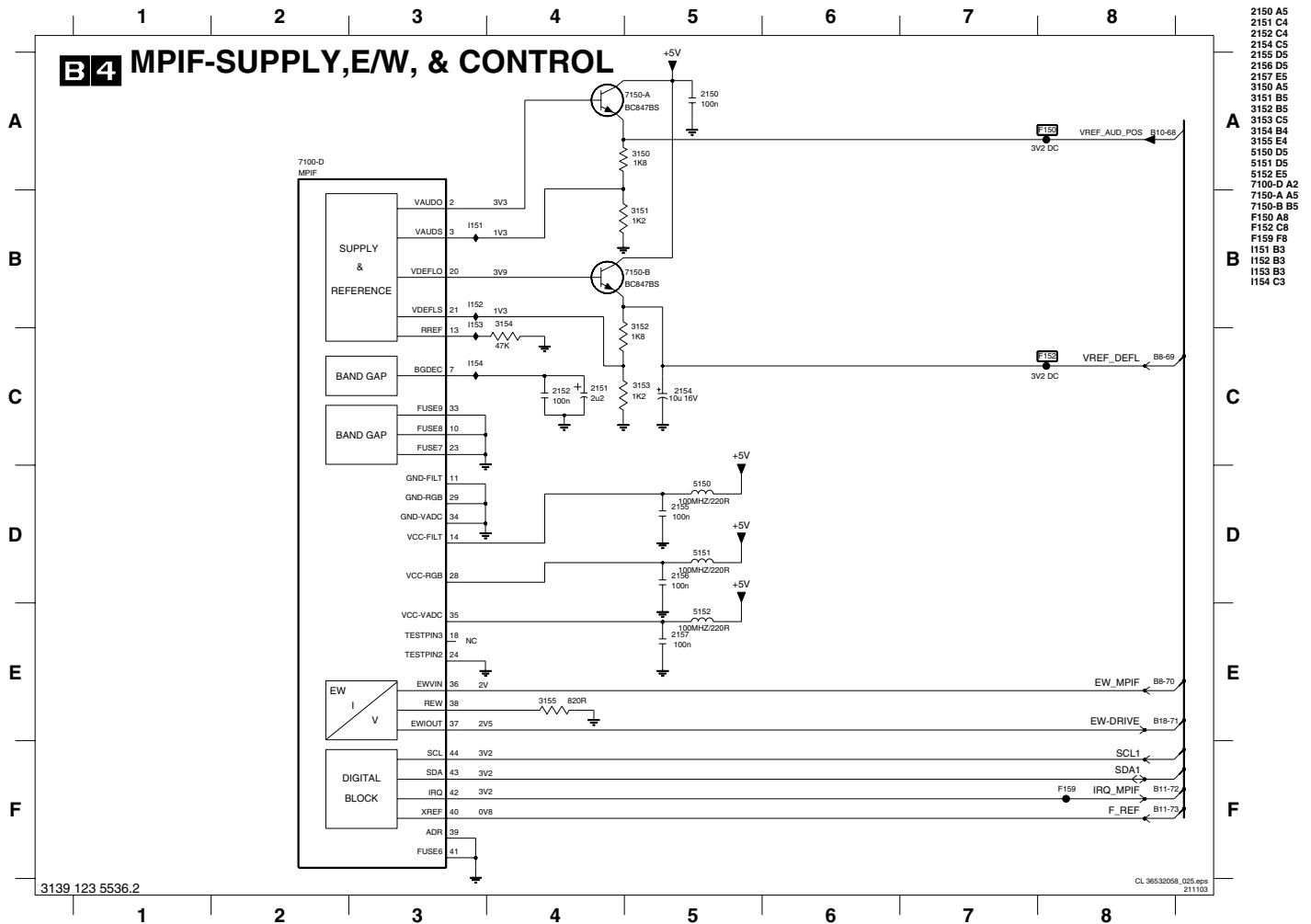




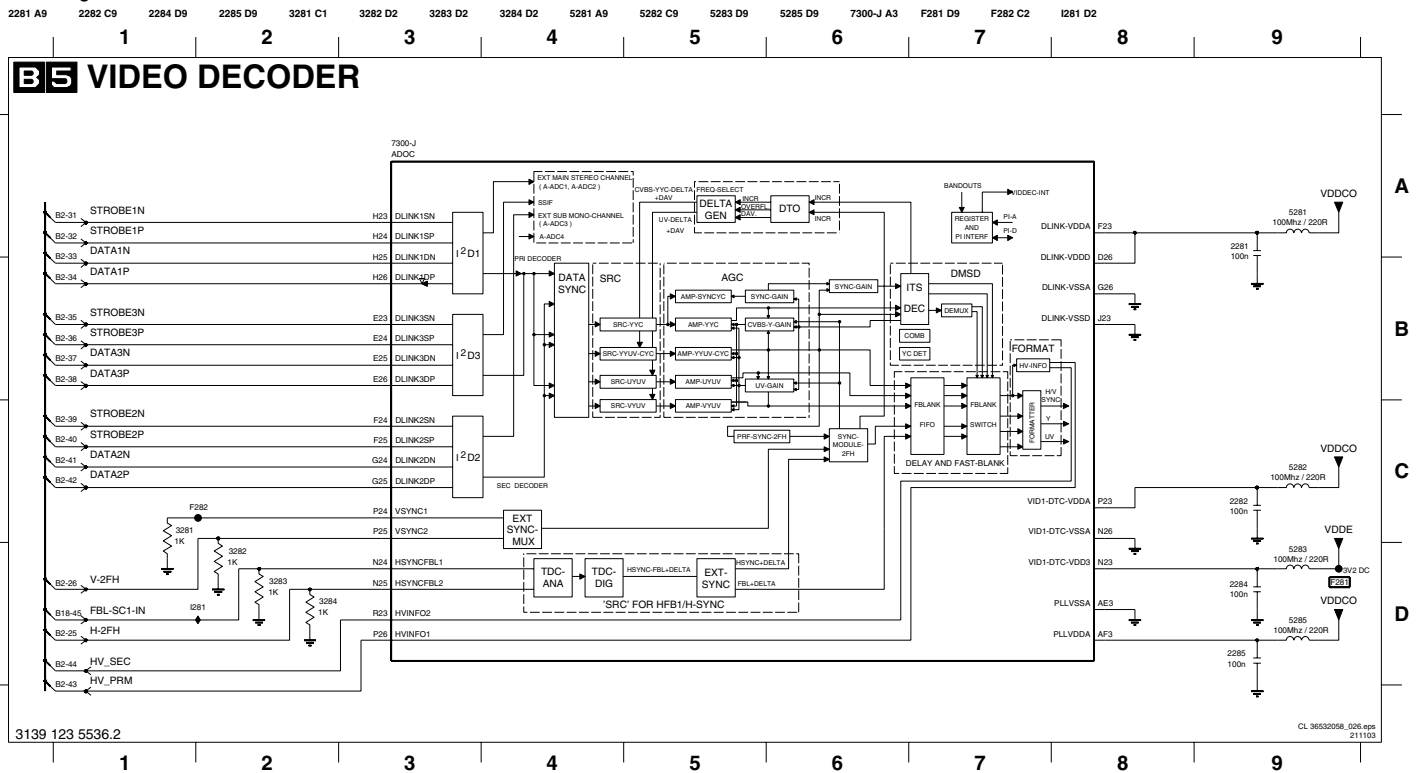
009 A8	2005 A8	2011 D1	2018 C2	2027 E2
117 E1	2006 A8	2012 B2	2019 C2	2028 E2
118 B9	2007 B2	2013 C2	2021 D2	2029 A10
002 A9	2008 B2	2014 C3	2022 D2	2030 D9
003 A9	2009 C1	2015 C2	2024 D2	2031 C9
004 C1	2010 C1	2016 C2	2025 D2	2032 E9



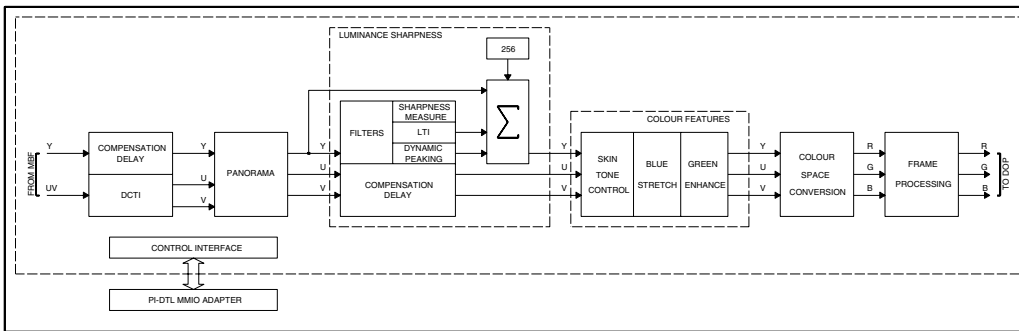
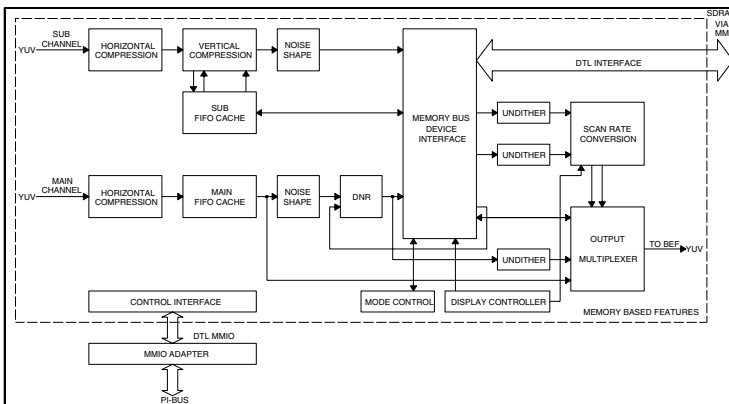
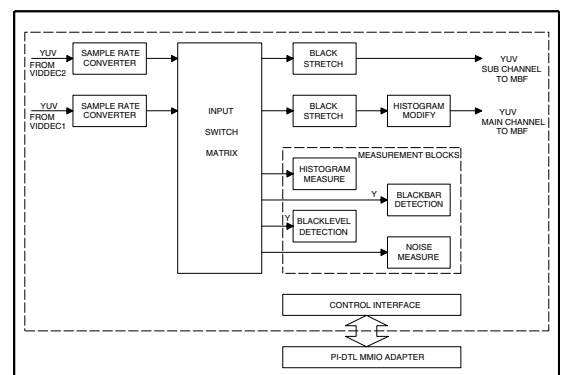
## Small Signal Board: MPIF-Supply, E/W, &amp; Control



## Small Signal Board: Video Decoder



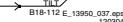
## Small Signal Board: Feature Box

**B6 FEATURE BOX**7300  
BACK END PROCESSING7300  
MEMORY BASED PROCESSING7300  
FRONT END PROCESSING

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CL 36532058\_027.apr  
02/06/03

2300 B1	2311 A9	2324 D4	2329 B8	2303 D7	2308 A5	2313 A8	2320 B8	2326 D4	2332 D8	2337 B4	2347 D6	5307 A5	6326 D4	7303 D8	7320 B9 A8	I901 C5	I906 A6
2305 E6	2317 B6	2325 C5	2331 C9	2304 D7	2308 A8	2316 B8	2321 C8	2328 C5	2333 D8	2338 D8	2348 D6	5317 B5	6327 E5	7304 D7	7330 A9 D8	I902 C6	I907 A5
2309 A4	2318 B5	2326 C6	2339 D6	2305 E7	2310 A8	2317 A5	2322 C8	2329 C8	2334 A4	2339 A5	2349 C6	5327 B5	6330 H A1 A	7310 A9 A8	7340 B9 D8	I903 D4	I908 A6
2310 A5	2321 B6	2346 E6	2331 C9	2308 A8	2316 B8	2321 C8	2328 C5	2333 D8	2338 D8	2343 E6	2349 C6	5337 B5	6331 C5	7305 D8	7330 A9 A8	I904 C6	I909 A6
2310 A9	2328 B5	2332 B5	2302 B1	2307 A8	2313 A5	2317 A5	2322 C8	2329 D8	2334 A4	2339 A5	2349 C6	5300 A1	6301 E7	7302 C8	7320 A9 B8	I905 A5	I910 B6



2341 B2	2350 A7	2360 C6	2365 D7	2379 E10	3351 A7
2342 C2	2351 A8	2361 C8	2366 C10	3340 A2	3352 A9
2343 C2	2352 A9	2362 B9	2371 D9	3341 B2	3353 A9
2344 C1	2358 D7	2363 B7	2372 D9	3346 D2	3354 A10
2345 C1	2359 C6	2364 C8	2377 E10	3350 A8	3355 C6

2341 B2	2350 A7	2360 C6	2365 D7	2379 E10	3351 A7	3357 C7	3363 B9	3368 C10	3375 E9	4363 B8	5345 C1	6367 C10	7365 C8	F354 A9	I342 C6	I347 C8
2342 C1	2361 C8	2366 C10	2370 E12	3340 A2	3352 A7	3358 A6	3364 B9	3371 D9	3376 D8	4369 B9	6341 C1	6368 C9	F341 C3	F353 B8	I343 C6	I348 C10
2343 C2	2352 A9	2363 B9	2368 D8	3341 B2	3353 A8	3360 B8	3365 C8	3372 B8	3377 B8	4342 C2	6353 A9	6369 C9	F346 E5	F357 C7	I344 C7	I349 E10
2344 C1	2353 B9	2364 C9	2372 D9	3346 D2	3354 A10	3362 B8	3367 C8	3373 B8	3378 B8	4343 C3	6354 B9	6370 C9	F347 E6	F358 C8	I345 C7	I350 E10
2345 C1	2359 A9	2369 C9	2377 E10	3347 B2	3355 C8	3363 B9	3368 D9	3369 E10	3374 E9	4391 C3	6355 B9	6371 B8	F348 E6	F359 C8	I346 C6	I351 E10



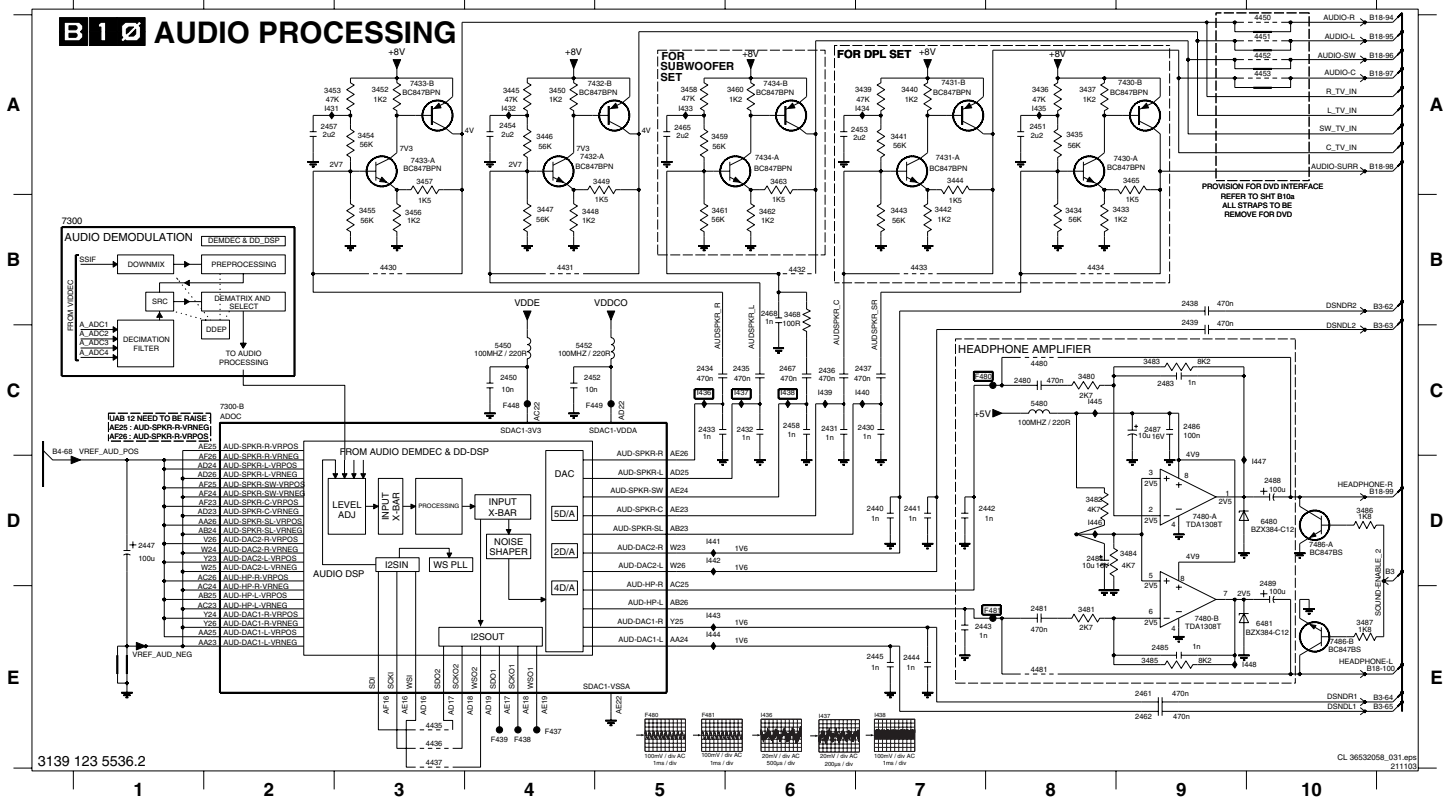
2380 B2	2395 D6	3382 A4	3386 B5	3391 E4	3394 D4	3397 C4	6382 A3	6397 C3	7382 A4	7393 D5	F383 C6	F386 B2	F390 C4	I382 C4
2386 B5	2397 D3	3384 E5	3388 C5	3392 E3	3395 E5	3398 C2	6384 B3	6398 C3	7383-A E5	F381 C6	F384 A4	F387 E4	F391 B4	
2395 E5	3387 D2	3385 B5	3390 C5	3393 D5	3396 D4	6381 A3	6385 A4	7300-G C6	7383-B B5	F382 C6	F385 B3	F389 C3	I381 A2	





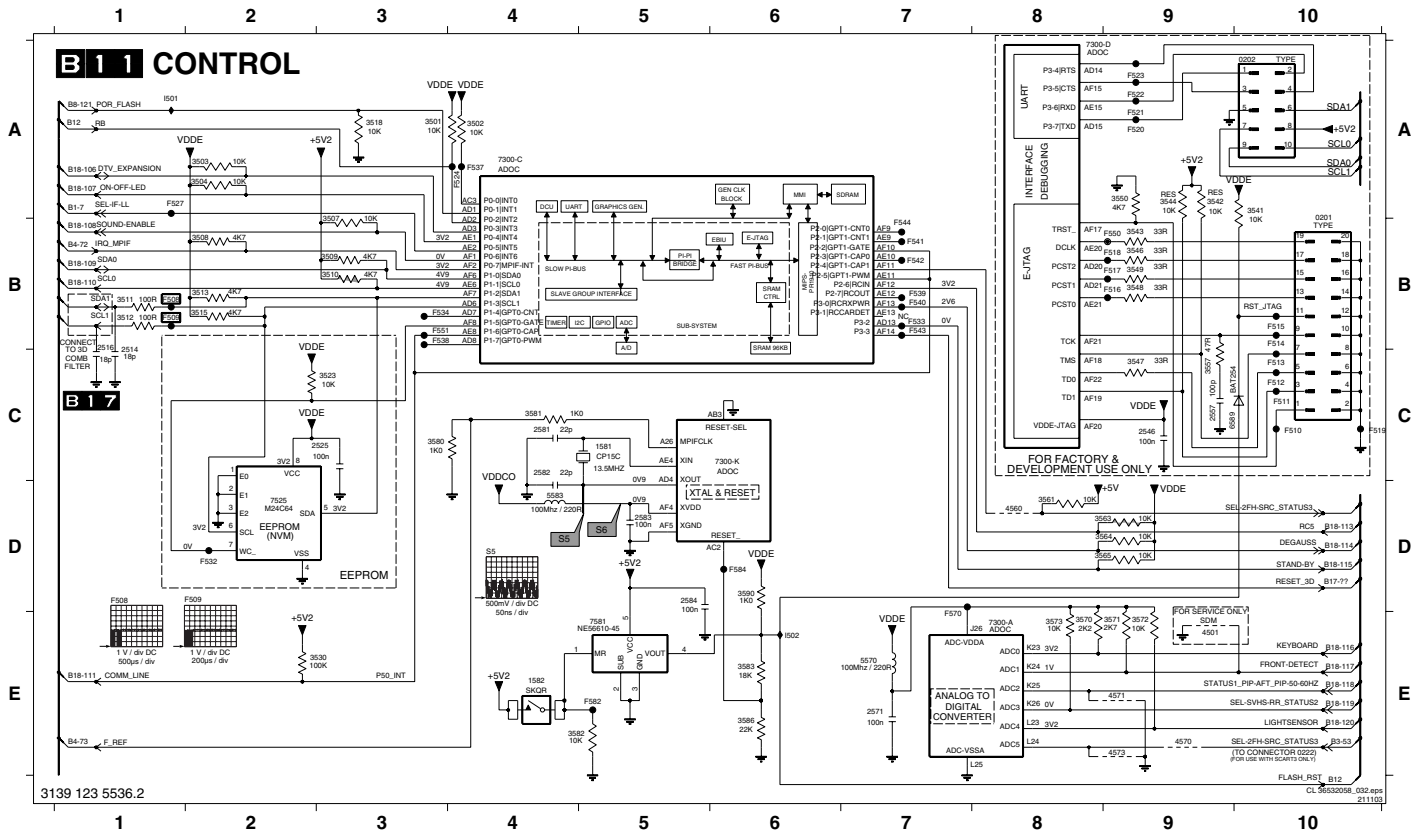
## Small Signal Board: Audio Processing

2430 C7	2437 C7	2444 E7	2454 A4	2468 B6	2487 C9	3437 A8	3445 A4	3453 A2	3460 A6	3481 E8	4430 B3	4437 E3	5450 C4	7430-B A9	7434-A A6	F438 E4	I432 A4	I439 C6	I446 D8
2431 C6	2438 B9	2445 E7	2457 A2	2480 C8	2488 D10	3439 A7	3446 A4	3454 A3	3461 B5	3482 D8	4431 B4	4450 A10	5452 C4	7431-A A7	7434-B A6	F439 E4	I433 A5	I440 C7	I447 D10
2432 C6	2439 B9	2447 D1	2458 C6	2481 E8	2489 D10	3440 A7	3447 B4	3455 B3	3462 B6	3483 C9	4432 B6	4451 A10	5480 C8	7431-B A7	7480-A D9	F448 C4	I434 A7	I441 D5	I448 E10
2433 C5	2440 D7	2450 C4	2461 E9	2483 C9	3433 B9	3441 A7	3448 B4	3456 B3	3463 A6	3484 D9	4433 B7	4452 A10	6480 D10	7432-A A4	7480-B E9	F449 C4	I435 A8	I442 D5	
2434 C5	2441 D7	2451 A8	2462 E9	2484 D8	3434 B8	3442 B7	3449 A5	3457 A3	3465 A9	3485 E9	4434 B8	4453 A10	6481 E10	7432-B A4	7480-A D10	F480 C7	I436 C5	I443 E5	
2435 C6	2442 D8	2452 C4	2463 A5	2485 E9	3435 A8	3443 B7	3450 A4	3458 A5	3468 B6	3486 D10	4435 E3	4480 C8	7300-B C2	7433-A A3	7486-B E10	F481 E8	I437 C6	I444 E5	
2436 C6	2443 E7	2453 A7	2467 C6	2486 C9	3436 A8	3444 A7	3452 A3	3459 A5	3480 C8	3487 E10	4436 E3	4481 E8	7430-A A8	7433-B A3	F437 E4	I431 A2	I438 C6	I445 C8	
1	2	3	4	5	6	7	8	9	10										

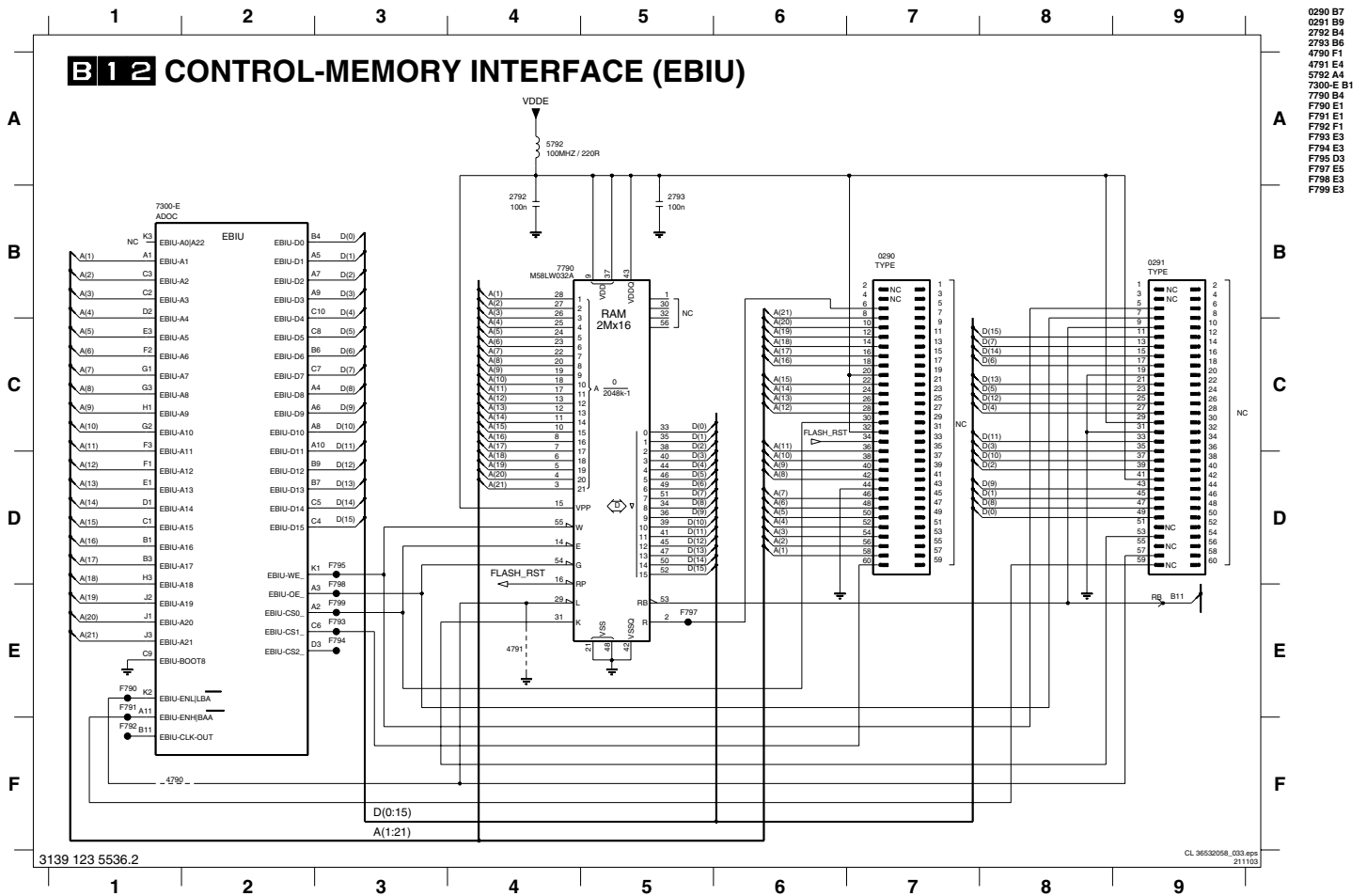


## Small Signal Board: Control

0201 A10	2525 C3	2583 D5	3507 B3	3513 B2	3542 A9	3549 B9	3565 D8	3581 C4	4560 D8	6589 C10	7581 E5	F513 C10	F519 C10	F527 A1	F539 B7	F550 B9	I502 E6
0202 A10	2546 C9	2584 D5	3508 B2	3515 B2	3543 B9	3550 A9	3570 E8	3582 E4	4570 E9	7300-A E8	F508 B1	F514 B10	F520 A9	F532 D2	F540 B7	F551 B3	
1581 C5	2557 C9	3501 A3	3509 B3	3518 A3	3544 A9	3557 C9	3571 E9	3583 E6	4571 E9	7300-C A4	F509 B1	F515 B10	F521 A9	F533 B7	F541 B7	F552 E7	
1582 E4	2571 E7	3502 A4	3510 B3	3523 C3	3546 B9	3561 D8	3572 E8	3586 E6	4573 E9	7300-D A8	F510 C10	F516 B9	F522 A9	F534 B3	F542 B7	F552 E5	
2514 B1	2581 C4	3503 A2	3511 B1	3530 E3	3547 C9	3563 D8	3573 E8	3590 D6	5570 E7	7300-K C5	F511 C10	F517 B9	F523 A9	F537 A4	F543 B7	F554 D6	
2516 C1	2582 C4	3504 A2	3512 B1	3541 A10	3548 B9	3564 D9	3580 C3	4501 E9	5583 D4	7525 D2	F512 C10	F518 B9	F524 A4	F538 B3	F544 B7	I501 A1	

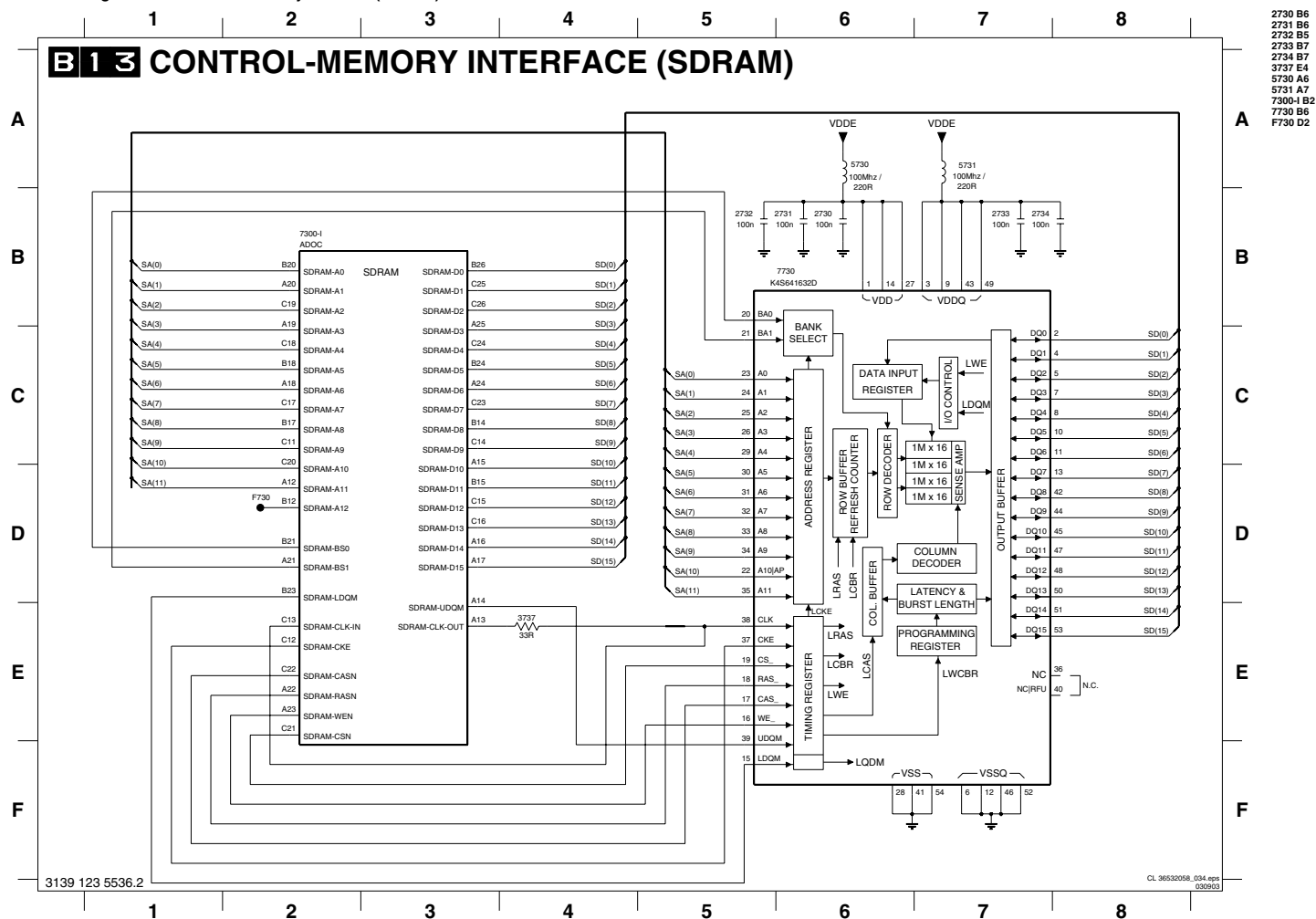


## Small Signal Board: Control-Memory Interface (EBIU)

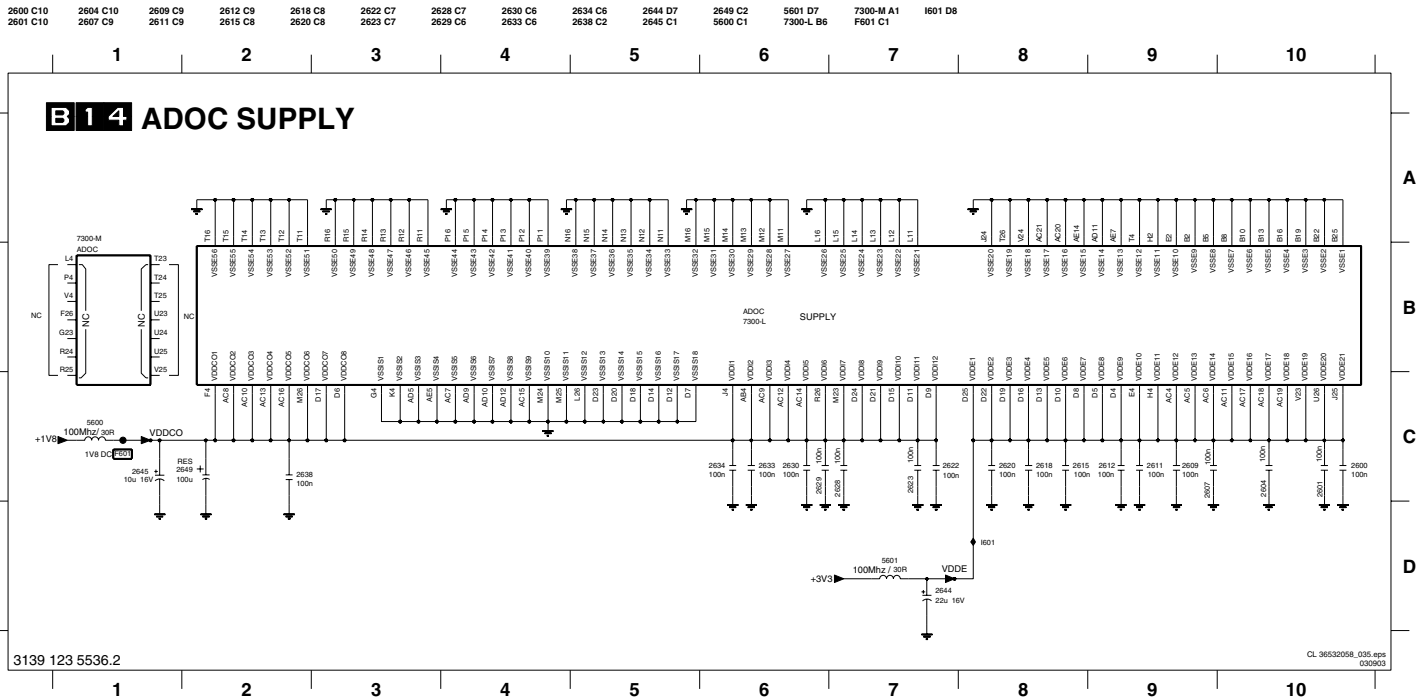


0290 B7  
0291 B9  
2792 B4  
2793 B6  
4790 F1  
4791 E4  
5792 A4  
7300-E B1  
7790 B4  
F790 E1  
F791 E1  
F792 F1  
F793 E3  
F794 E3  
F795 D3  
F797 E5  
F798 E3  
F799 E3

### B 1 3 CONTROL-MEMORY INTERFACE (SDRAM)

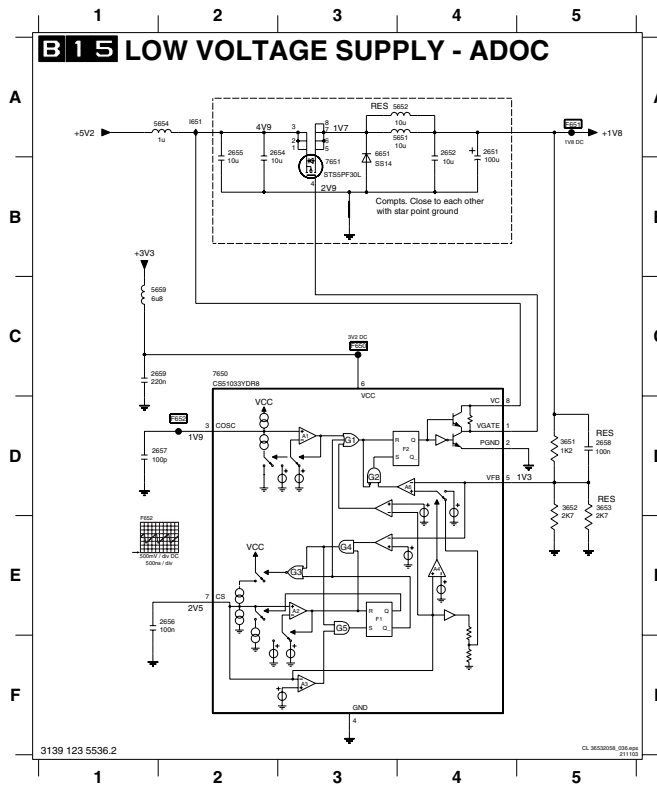


## Small Signal Board: ADOC Supply



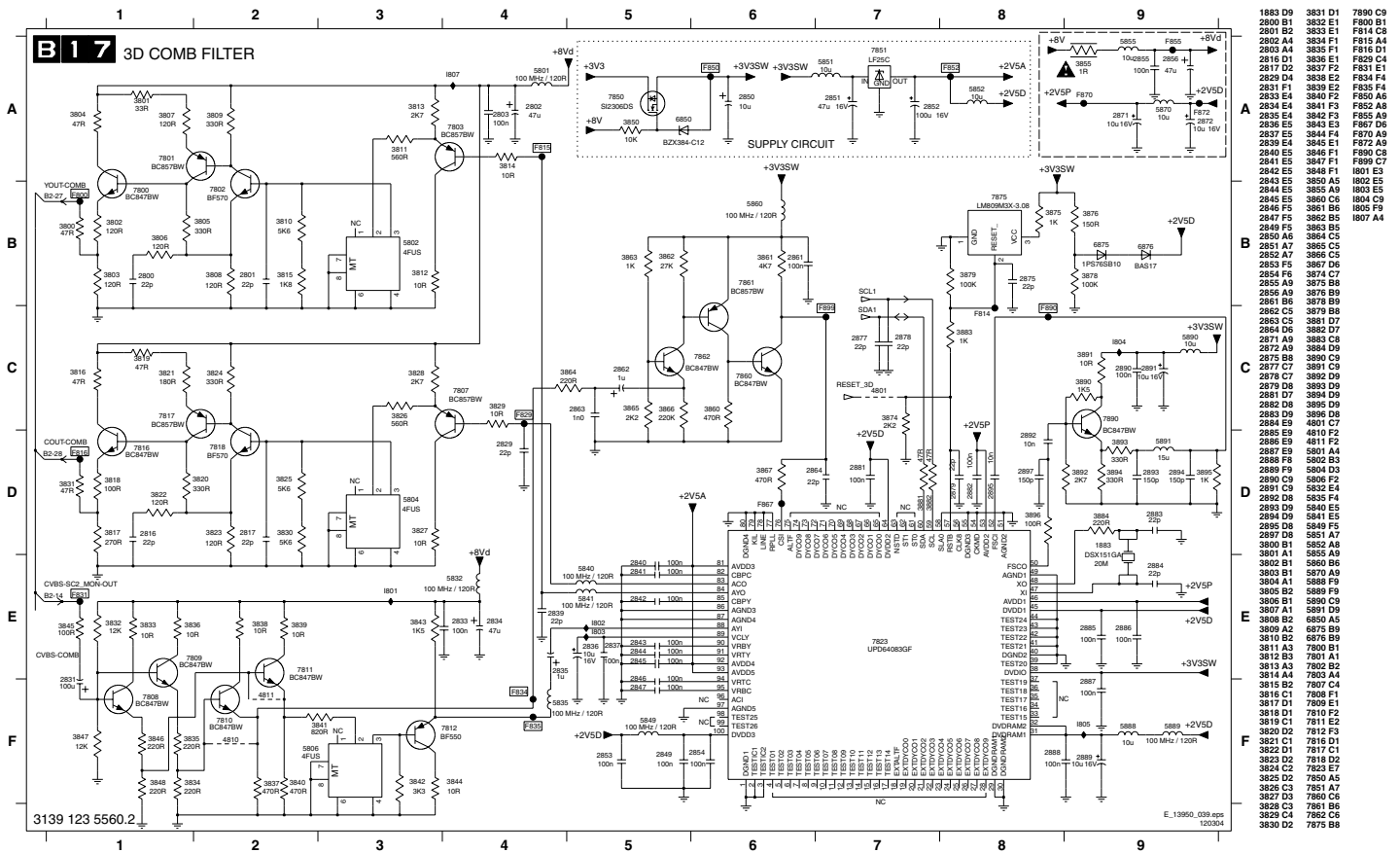
## Small Signal Board: Low Voltage Supply ADOC

## Personal Notes:



2651 A4  
2652 A4  
2654 A2  
2655 A2  
2656 E2  
2657 D2  
2658 D5  
2659 C2  
3651 D5  
3652 D5  
3653 D5  
5651 A4  
5652 A4  
5654 A2  
5659 C2  
7651 A3  
7652 C2  
7651 B3  
F650 C3  
F651 A5  
F652 D2  
6651 A2

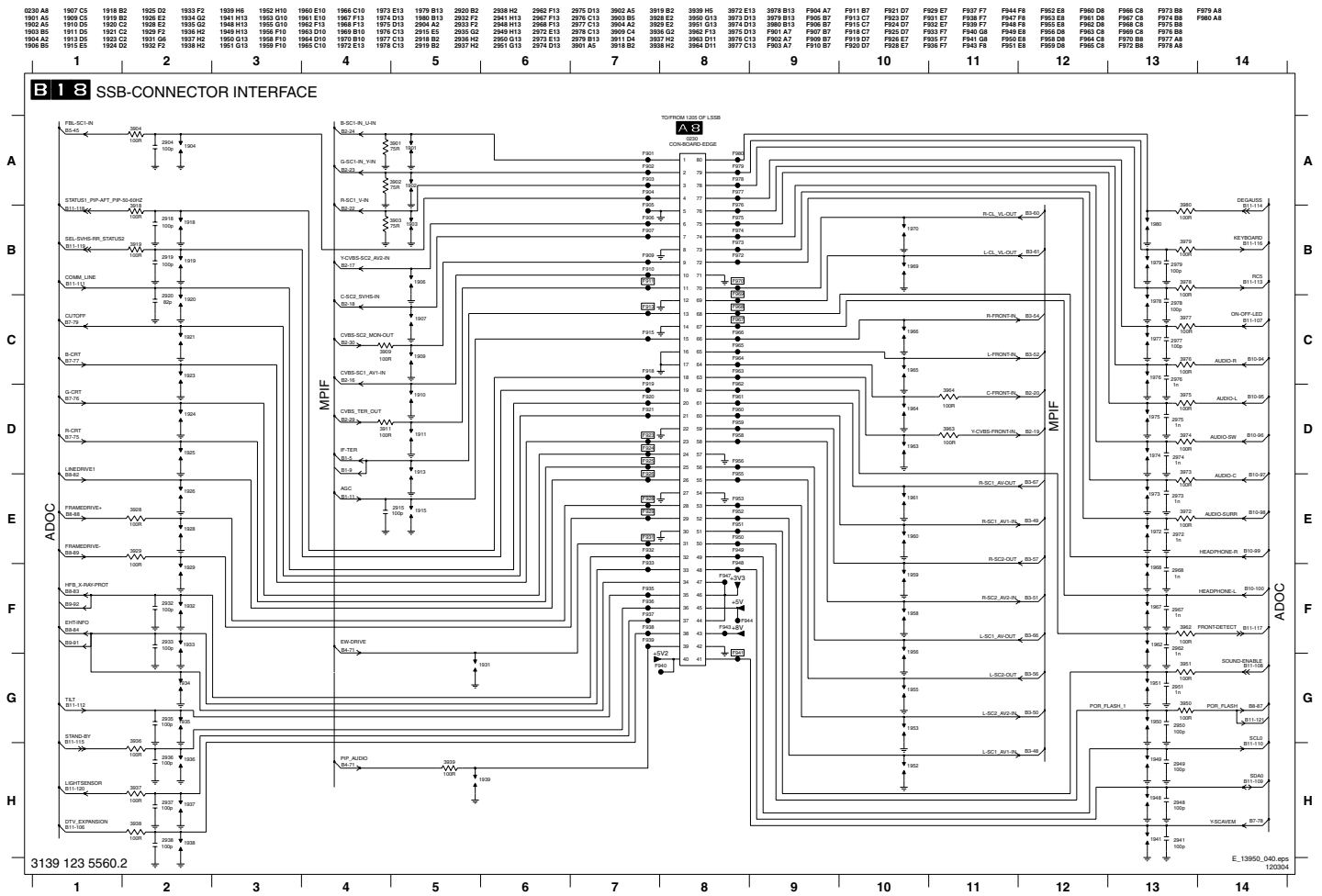
## Small Signal Board: 3D COMB Filter



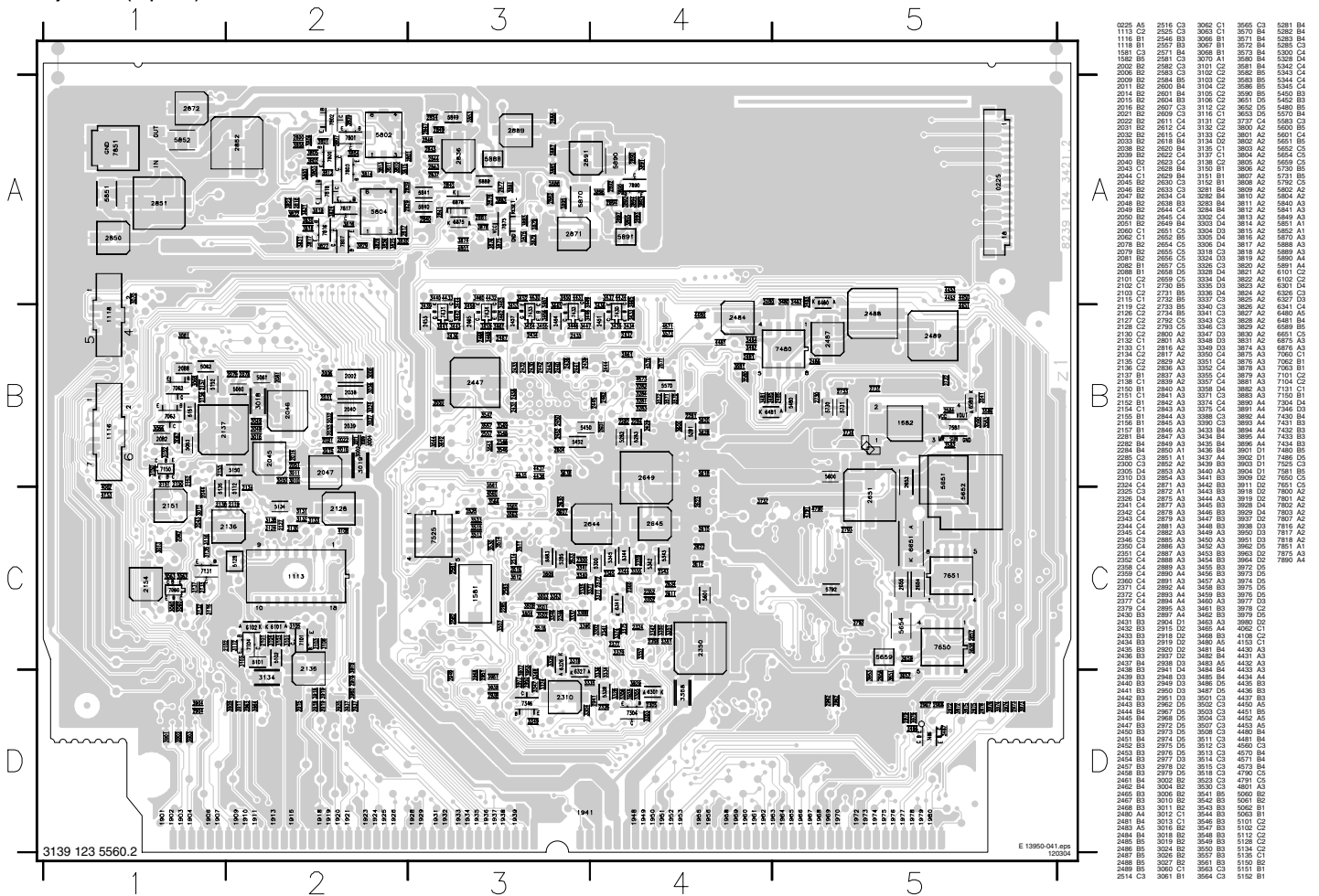
1883 D9 3831 D1 7890 C9  
2800 B1 3832 E1 F800 B1  
2901 B2 3833 E1 F814 C8  
2802 A4 3834 F1 F815 A4  
2803 A4 3835 F1 F816 D1  
2810 D1 3836 E1 F820 C4  
2817 D2 3837 F2 F831 E1  
2824 D4 3838 E2 F834 F4  
2831 F1 3839 E2 F835 F4  
2833 E4 3840 F2 F850 A6  
2835 E4 3841 F3 F852 A8  
2836 E4 3842 F3 F855 A9  
2836 C5 3843 C3 F867 D6  
2837 E5 3844 F4 F870 A9  
2839 E4 3845 E1 F872 A9  
2840 E5 3846 F1 F880 C8  
2841 E5 3847 F1 F899 C7  
2842 E5 3848 F1 B001 E3  
2843 E5 3850 A5 B002 E5  
2844 E5 3855 A9 B003 E5  
2845 E5 3860 C5 B004 C9  
2846 F5 3861 B6 B005 F9  
2847 F5 3862 B5 B007 A4  
2848 F5 3863 B5  
2850 A6 3864 C5  
2851 A7 3865 C5  
2852 A7 3866 C5  
2853 A9 3875 B9  
2854 F6 3874 C7  
2855 A9 3875 B6  
2856 A9 3875 B9  
2861 B6 3878 B9  
2862 C5 3879 B9  
2863 C5 3881 D7  
2864 D6 3882 D7  
2867 A9 3883 C9  
2872 A9 3884 D9  
2873 D8 3885 D9  
2874 D9 3886 D9  
2875 B9 3890 C9  
2877 C7 3891 C9  
2878 C7 3892 D9  
2879 D8 3893 D9  
2880 D8 3894 D9  
2881 D8 3895 D9  
2882 D8 3896 D9  
2883 D9 3896 D9  
2884 E9 4801 C7  
2885 E9 4810 F2  
2886 E9 4811 F2  
2887 E9 5001 A4  
2888 F8 5002 B3  
2889 F9 5003 D3  
2890 C9 5005 F2  
2891 C9 5032 E4  
2892 D8 5033 F4  
2893 D9 5040 E5  
2894 D9 5041 E5  
2895 D8 5049 F5  
2897 D8 5051 A7  
2898 B1 5052 A8  
2899 B1 5055 A9  
2900 B1 5060 B6  
2901 B2 5070 A9  
2902 A1 5088 F9  
2903 B2 5089 F9  
2906 B1 5090 C9  
2907 A1 5091 D9  
2908 B2 5090 A5  
2909 A2 5095 B9  
2910 B2 5095 B9  
2911 A3 7800 B1  
2912 B3 7801 A1  
2913 A3 7802 B2  
2914 A4 7803 A4  
2915 B2 7807 C4  
2916 C1 7808 F1  
2917 D1 7809 E1  
2918 D1 7810 F2  
2919 C1 7811 E2  
2920 D2 7812 F3  
2921 C1 7816 D1  
2922 D1 7817 C1  
2923 D2 7818 D2  
2924 C2 7823 E7  
2925 D2 7850 A5  
2926 C3 7851 A7  
2927 D3 7860 C6  
2928 C3 7861 B6  
2929 C4 7862 C6  
2930 D2 7875 B6



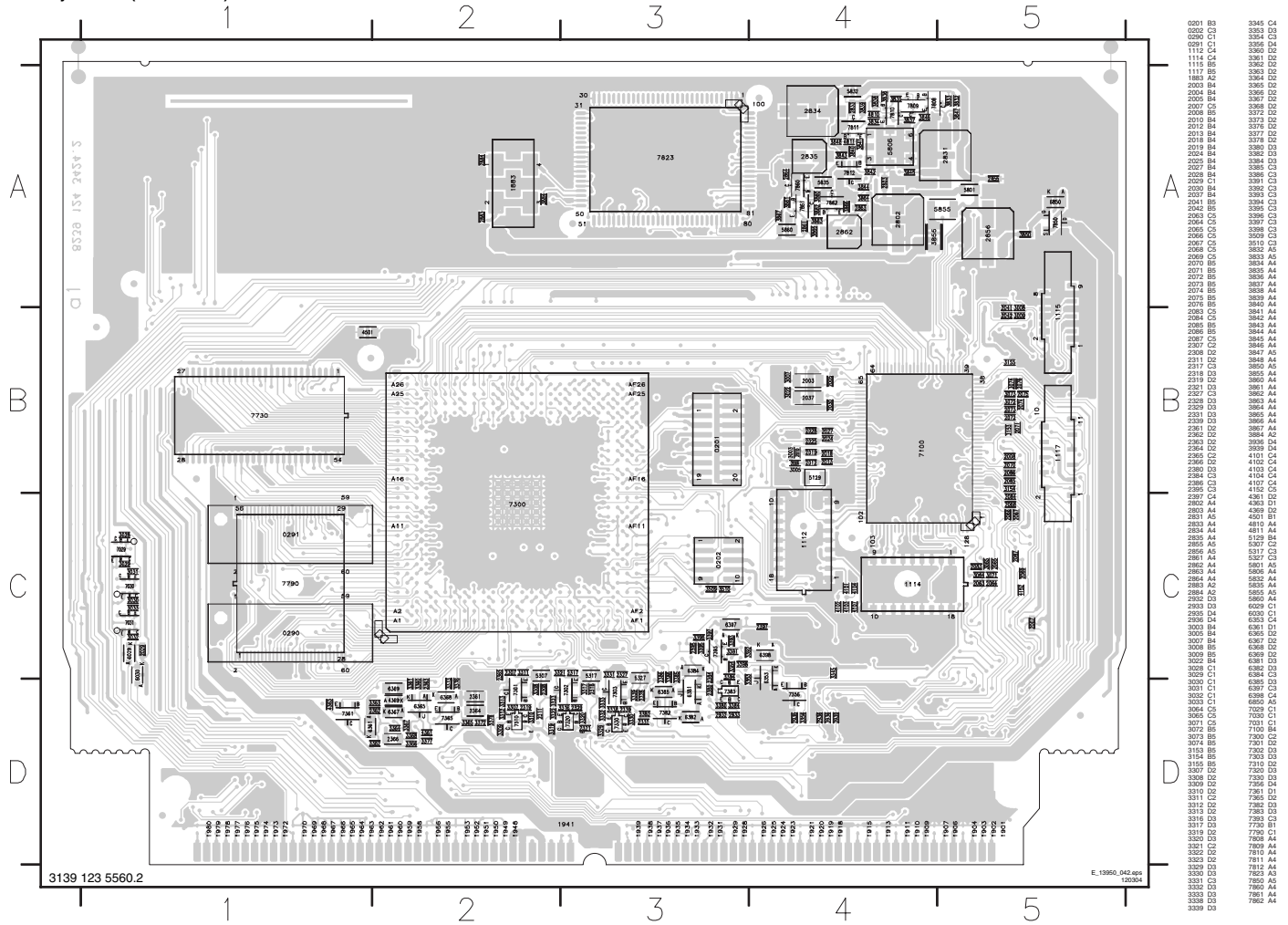
## Small Signal Board: Connector Interface



Layout SSB (Top Side)



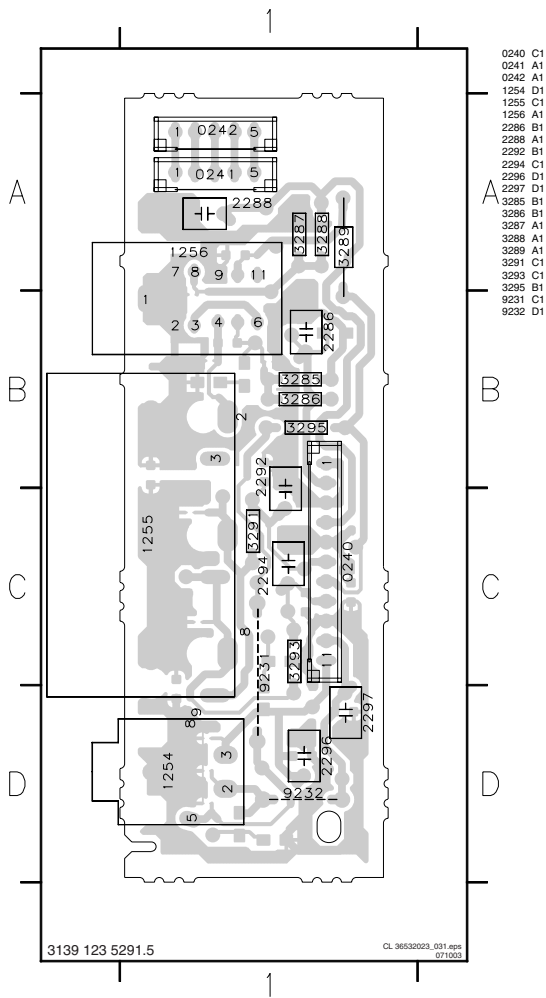
Layout SSB (Bottom Side)



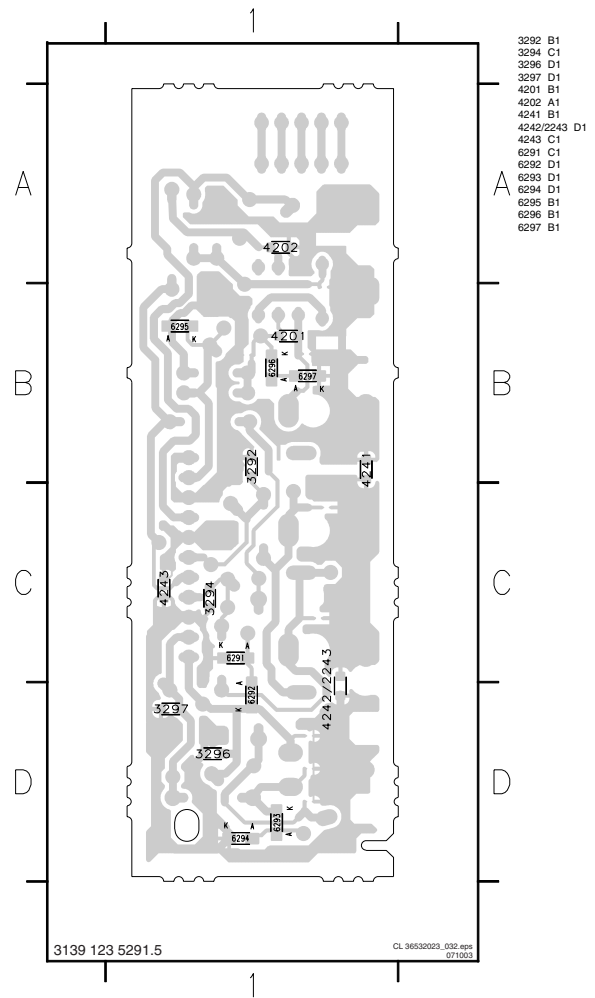
0001 B3 3340 C4  
0002 C1 3351 D3  
0003 C1 3352 D4  
0004 C1 3353 D4  
0005 C1 3354 D4  
0006 C1 3355 D4  
0007 C1 3356 D4  
0008 C1 3357 D4  
0009 C1 3358 D4  
0010 C1 3359 D4  
0011 C1 3360 D4  
0012 C1 3361 D4  
0013 C1 3362 D4  
0014 C1 3363 D4  
0015 C1 3364 D4  
0016 C1 3365 D4  
0017 C1 3366 D4  
0018 C1 3367 D4  
0019 C1 3368 D4  
0020 C1 3369 D4  
0021 C1 3370 D4  
0022 C1 3371 D4  
0023 C1 3372 D4  
0024 C1 3373 D4  
0025 C1 3374 D4  
0026 C1 3375 D4  
0027 C1 3376 D4  
0028 C1 3377 D4  
0029 C1 3378 D4  
0030 C1 3379 D4  
0031 C1 3380 D4  
0032 C1 3381 D4  
0033 C1 3382 D4  
0034 C1 3383 D4  
0035 C1 3384 D4  
0036 C1 3385 D4  
0037 C1 3386 D4  
0038 C1 3387 D4  
0039 C1 3388 D4  
0040 C1 3389 D4  
0041 C1 3390 D4  
0042 C1 3391 D4  
0043 C1 3392 D4  
0044 C1 3393 D4  
0045 C1 3394 D4  
0046 C1 3395 D4  
0047 C1 3396 D4  
0048 C1 3397 D4  
0049 C1 3398 D4  
0050 C1 3399 D4  
0051 C1 3400 D4  
0052 C1 3401 D4  
0053 C1 3402 D4  
0054 C1 3403 D4  
0055 C1 3404 D4  
0056 C1 3405 D4  
0057 C1 3406 D4  
0058 C1 3407 D4  
0059 C1 3408 D4  
0060 C1 3409 D4  
0061 C1 3410 D4  
0062 C1 3411 D4  
0063 C1 3412 D4  
0064 C1 3413 D4  
0065 C1 3414 D4  
0066 C1 3415 D4  
0067 C1 3416 D4  
0068 C1 3417 D4  
0069 C1 3418 D4  
0070 C1 3419 D4  
0071 C1 3420 D4  
0072 C1 3421 D4  
0073 C1 3422 D4  
0074 C1 3423 D4  
0075 C1 3424 D4  
0076 C1 3425 D4  
0077 C1 3426 D4  
0078 C1 3427 D4  
0079 C1 3428 D4  
0080 C1 3429 D4  
0081 C1 3430 D4  
0082 C1 3431 D4  
0083 C1 3432 D4  
0084 C1 3433 D4  
0085 C1 3434 D4  
0086 C1 3435 D4  
0087 C1 3436 D4  
0088 C1 3437 D4  
0089 C1 3438 D4  
0090 C1 3439 D4  
0091 C1 3440 D4  
0092 C1 3441 D4  
0093 C1 3442 D4  
0094 C1 3443 D4  
0095 C1 3444 D4  
0096 C1 3445 D4  
0097 C1 3446 D4  
0098 C1 3447 D4  
0099 C1 3448 D4  
0100 C1 3449 D4



Layout Side I/O Panel (Top Side)



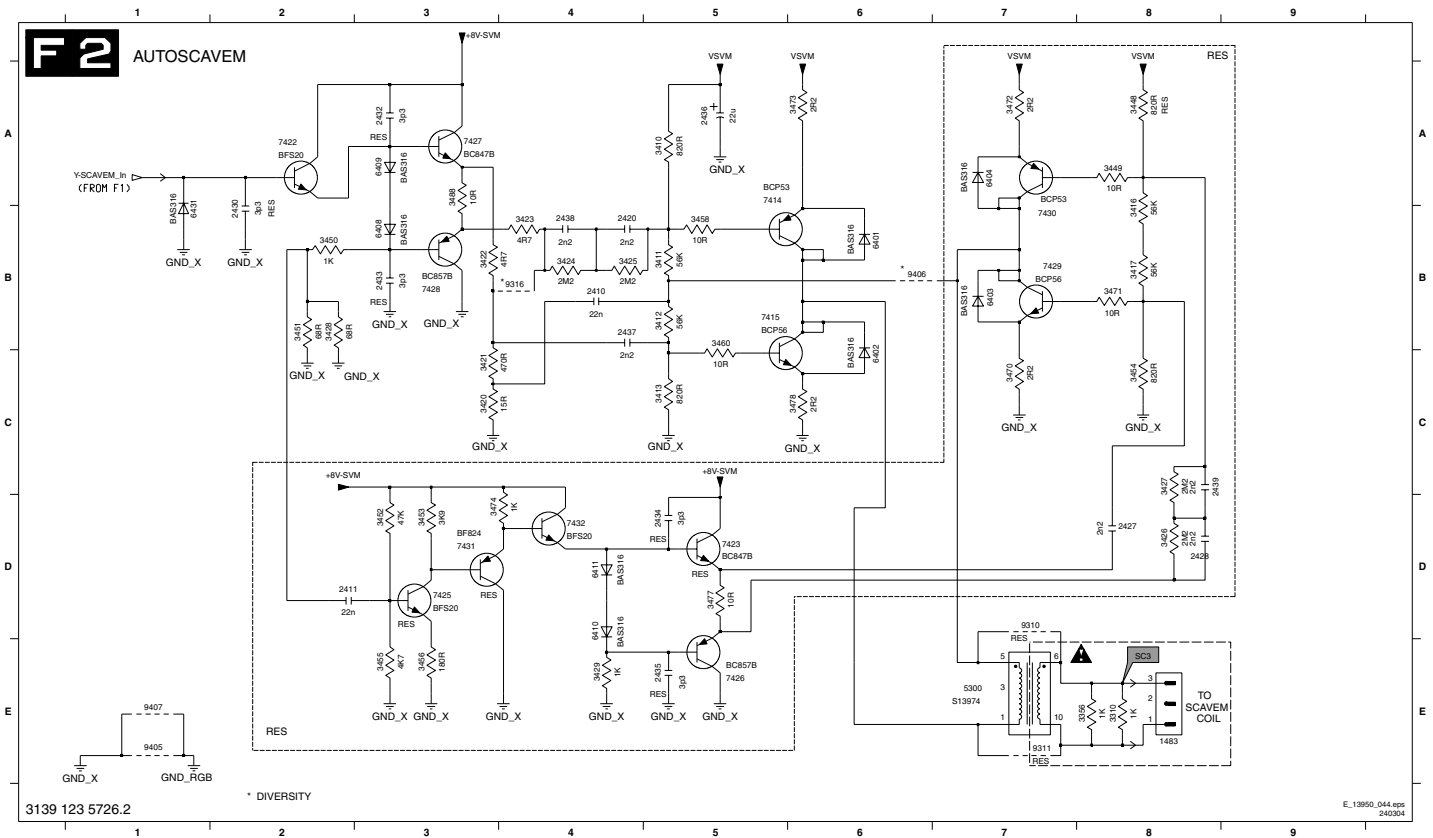
Layout Side I/O Panel (Bottom Side)





## CRT Panel: Auto SCAVEM

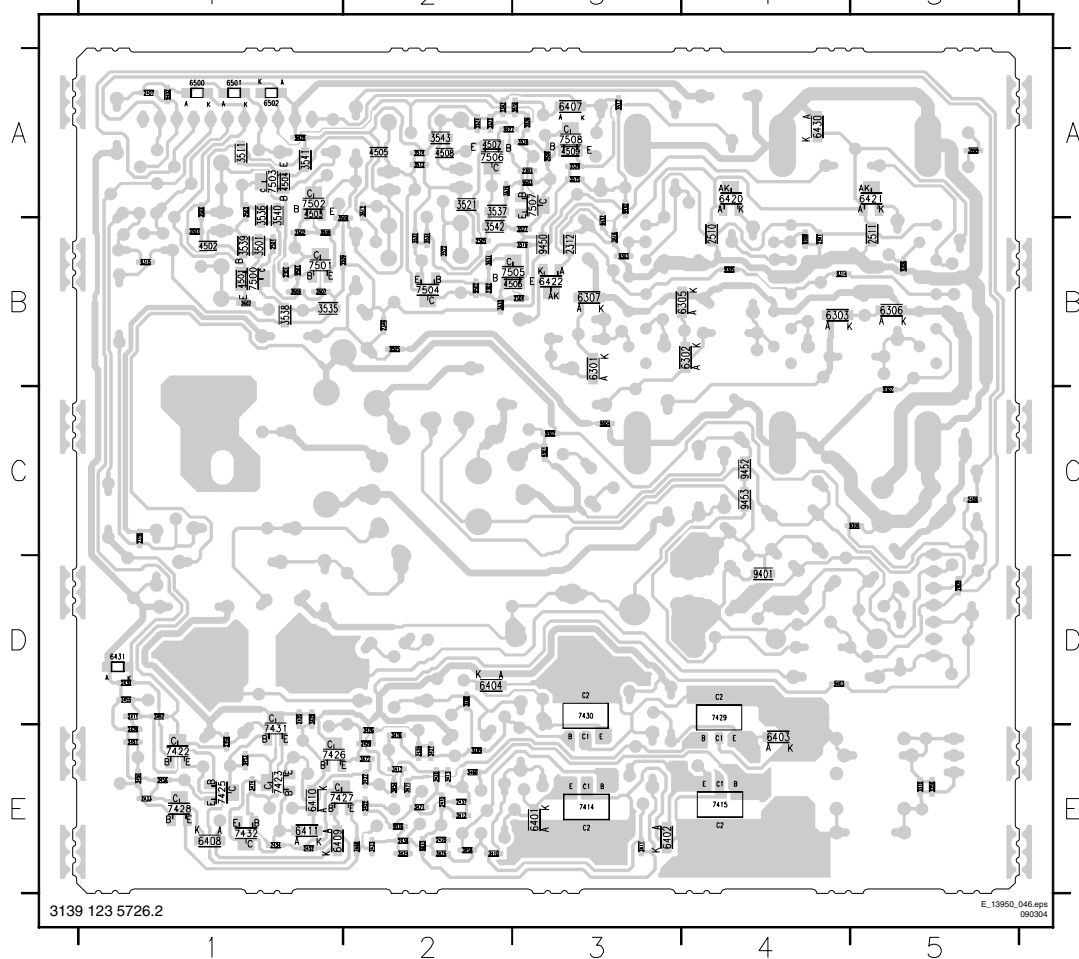
1483 E8 2430 B2 2437 B4 3411 B5 3421 C3 3427 C8 3451 B2 3458 B5 3474 D3 6402 C5 6411 D4 7425 D3 7431 D3 9406 B6  
 2410 B4 2432 A3 2438 B4 3412 B5 3422 B3 3428 B2 3452 D3 3460 B5 3477 D5 6403 B7 6431 B1 7426 E5 7432 D4 9407 E1  
 2411 D2 2433 B3 2439 C8 3413 C5 3423 B4 3429 E4 3453 D3 3470 C7 3478 C6 6404 A7 7414 A5 7427 A3 9310 D7  
 2420 B4 2434 D5 3310 E8 3416 B8 3424 B4 3448 A8 3454 C8 3471 B8 3488 A3 6408 B3 7415 B5 7428 B3 9311 E7  
 2427 D8 2435 E5 3356 E8 3417 B8 3425 B4 3449 A8 3455 E3 3472 A7 5300 E7 6409 A3 7422 A2 7429 B7 9316 B4  
 2428 D8 2436 A5 3410 A5 3420 C3 3426 D8 3450 B2 3456 E3 3473 A6 6401 B6 6410 D4 7423 D5 7430 B7 9405 E1



0031 B1	5400 D1
0033 B2	5500 B5
0035 B3	5501 A4
1237 C4	5502 A4
1298 D4	6400 D3
1424 D1	6405 D2
1434 C5	6406 A3
1435 D3	6426 B2
1483 E1	6427 B1
1940 A5	6428 B3
2133 C1	7330 B3
2137 C5	7340 B1
2319 C2	7350 B2
2324 B5	9304 B3
2338 B2	9309 B2
2339 B3	9310 E1
2340 B3	9311 E1
2347 B5	9405 D5
2352 C2	9406 E3
2358 E5	9407 A5
2403 C2	9416 D1
2404 C2	9417 E3
2405 C2	9418 D4
2436 E4	9419 D5
3301 D5	9423 A5
3303 D4	9424 B4
3304 C3	9430 A4
3305 A5	9431 C1
3334 B5	9435 A2
3338 B3	9436 B5
3339 C3	9451 C2
3340 C3	9506 D5
3341 D1	
3345 D2	
3346 D5	
3347 C5	
3348 D5	
3349 C5	
3350 B2	
3351 B1	
3352 B3	
3401 D1	
3402 C1	
3403 D2	
3404 D2	
3470 D3	
3472 E3	
3473 E4	
3478 E3	
3510 A3	
3520 A1	
3530 A2	
3541 B1	
5300 E1	
5303 C5	
5304 C2	
5308 B5	
5309 D1	
5310 D1	



1                      2                      3                      4                      5

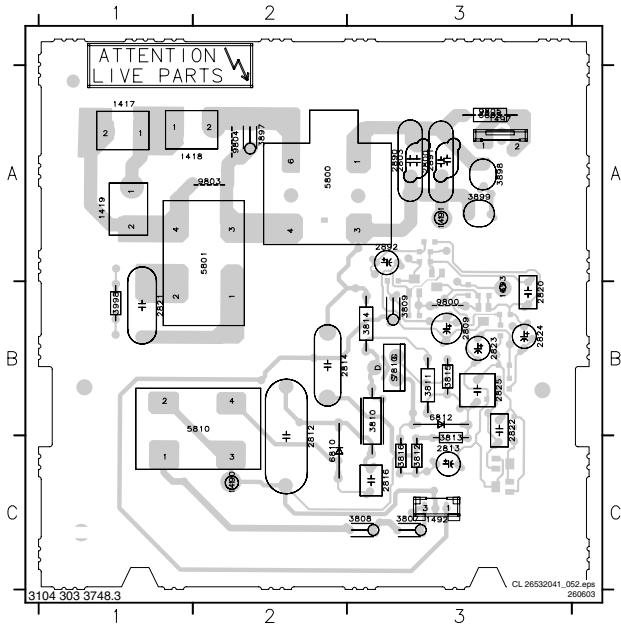


2301	B1	3456	E1	6303	B4	9432	E2
2302	B2	3458	E2	6305	B4	9437	B3
2303	A3	3460	E2	6306	B5	9450	B3
2312	B3	3471	E2	6307	B3	9452	C4
2318	C1	3474	E1	6401	E3	9453	C4
2341	B4	3477	E2	6402	E3	9501	B1
2342	A2	3488	E2	6403	E4	9502	B2
2348	B2	3501	B1	6404	D2	9503	A3
2359	E1	3502	B1	6407	A3	9504	C3
2407	A1	3503	B1	6408	E1	9505	B2
2408	C5	3504	A1	6409	E1		
2409	D5	3505	B1	6410	E1		
2410	E2	3506	B1	6411	E1		
2411	D1	3507	B1	6420	A4		
2420	E2	3508	B1	6421	A5		
2427	E2	3509	B1	6422	B3		
2428	E2	3511	A1	6430	A4		
2430	D1	3512	A2	6431	D1		
2432	E5	3513	A3	6500	A1		
2433	E1	3514	A2	6501	A1		
2434	E1	3515	A3	6502	E1		
2435	D1	3516	B3	7414	E3		
2437	E3	3517	A3	7415	E4		
2438	E2	3518	A3	7422	E1		
2439	E2	3519	B3	7423	E1		
2501	B1	3521	A2	7425	E1		
2502	B1	3522	B2	7426	E1		
2503	A1	3523	A2	7427	E1		
2504	B3	3524	A2	7428	E1		
2505	B2	3525	A2	7429	D4		
2506	A3	3526	A3	7430	D3		
2510	B4	3527	B3	7431	E1		
2511	B5	3528	A3	7432	E1		
3310	C5	3529	A3	7500	B1		
3356	E5	3531	B2	7501	B1		
3410	E2	3532	B2	7502	E1		
3411	C3	3533	B2	7503	A1		
3412	E2	3534	B2	7504	B2		
3413	E2	3535	B1	7505	B3		
3416	E2	3536	A1	7506	E2		
3417	E2	3537	A2	7507	A3		
3420	E2	3538	B1	7508	A3		
3421	E2	3539	B1	9300	C5		
3422	E2	3540	A1	9301	C3		
3423	E2	3541	A1	9302	C3		
3424	E2	3542	B2	9303	B3		
3425	E2	3543	A2	9305	B4		
3426	E2	3999	A5	9306	B5		
3427	E2	4501	B1	9307	C5		
3428	E1	4502	B1	9308	B4		
3429	D1	4503	A1	9314	B1		
3448	D2	4504	A1	9315	B1		
3449	E2	4505	A2	9316	B1		
3450	E1	4506	B3	9401	D4		
3451	E1	4507	A2	9402	A1		
3452	D1	4508	A2	9403	D4		
3453	E1	4509	A3	9427	A2		
3454	E2	6301	B3	9428	A1		
3455	D1	6302	B4	9432	A3		



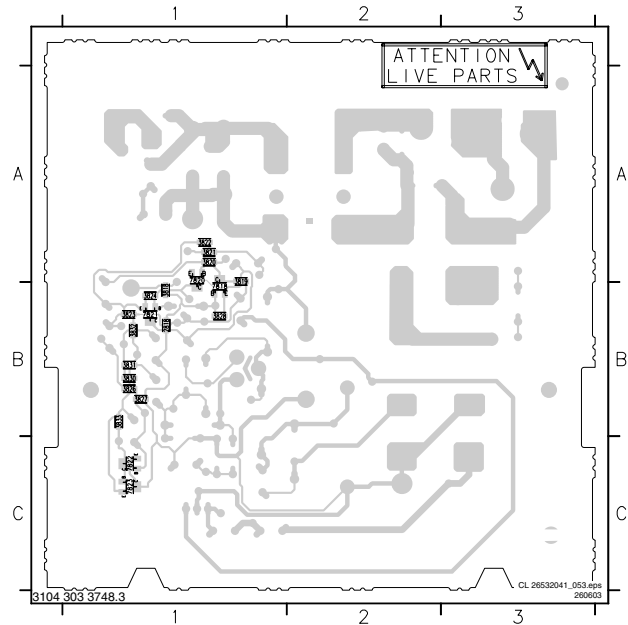
VDAF +  
2ND ORDERS[illegible]

Layout VDAF + 2ND Order Panel (Top Side)



1417 A1  
1418 A1  
1419 A1  
1490 C2  
1491 A3  
1492 C3  
1497 A3  
1693 B3  
2800 A3  
2803 A3  
2809 B3  
2812 C2  
2813 C3  
2814 B2  
2816 C3  
2820 B3  
2821 B1  
2822 B3  
2823 B3  
2824 B3  
2825 B3  
2890 A3  
2891 A3  
2892 A3  
3805 A3  
3807 C3  
3808 C3  
3809 B3  
3810 B3  
3811 B3  
3812 C3  
3813 C3  
3814 B3  
3815 B3  
3816 C3  
3897 A2  
3898 A3  
3899 A3  
3998 B1  
5800 A2  
5801 A1  
5810 B2  
6810 C2  
6812 B3  
7810 B3  
9800 B3  
9803 A2  
9804 A2  
9805 A3

Layout VDAF + 2ND Order Panel (Bottom Side)

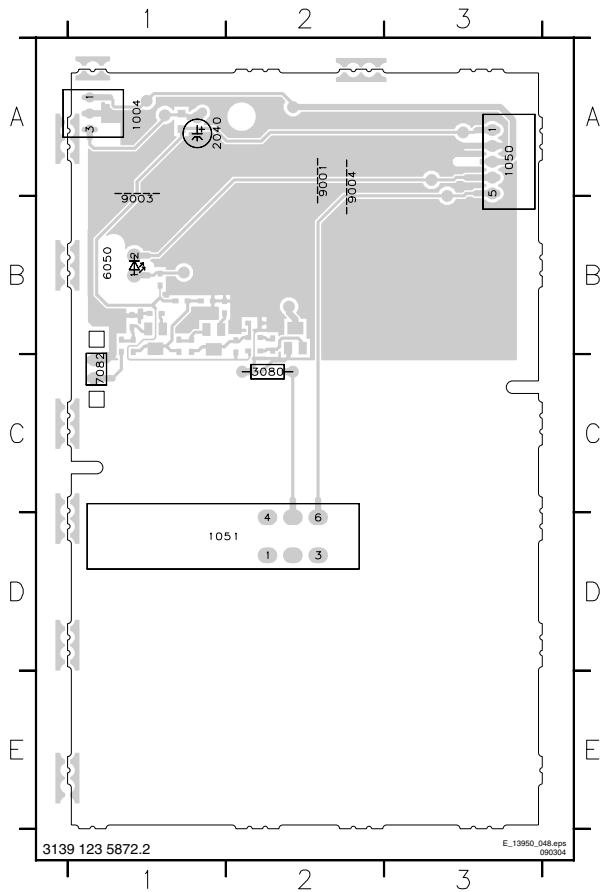


2818 B1  
3818 B1  
3819 A1  
3820 A1  
3821 A1  
3822 A1  
3823 B1  
3824 B1  
3826 B1  
3827 B1  
3828 B1  
3830 B1  
3831 B1  
3832 B1  
3833 B1  
7818 B1  
7820 A1  
7821 B1  
7822 C1  
7823 C1

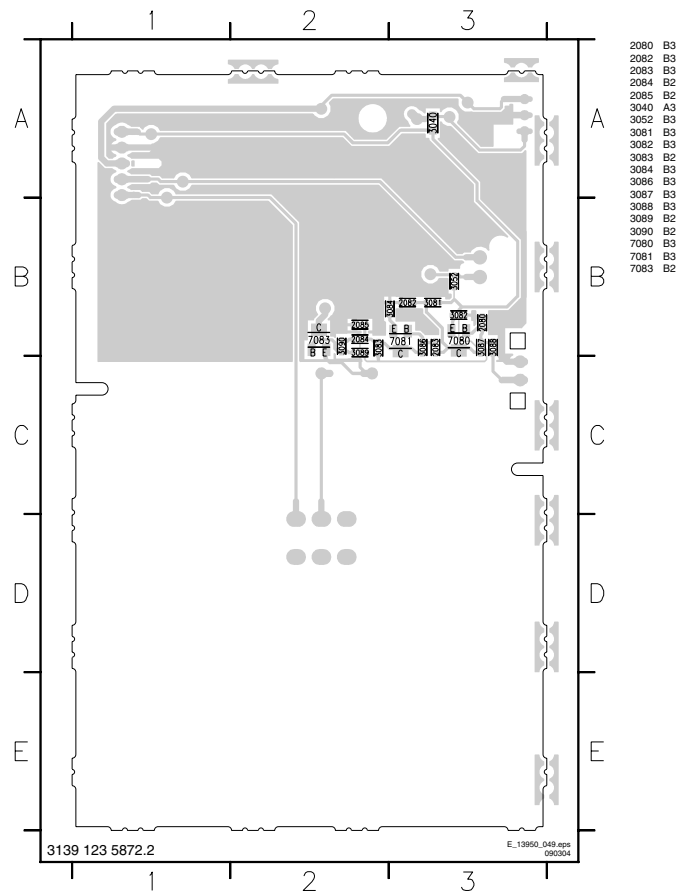
1004 C2  
1050 C2  
1051 C3  
2040 E4  
2080 F1  
2082 F2  
2083 E2  
2084 E3  
2085 E3  
3040 D4  
3052 B3  
3080 C3  
3081 E1  
3082 F2  
3083 E3  
3084 F2  
3086 E2  
3087 E1  
3088 F1  
3089 E3  
3090 E3  
6050 B3  
7080 F1  
7081 E2  
7082 F1  
7083 E4

Blank lined paper for writing.

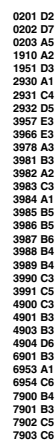
Layout Front Interface Panel FL13 Styling (Top Side)



Layout Front Interface Panel FL3 Styling (Bottom Side)

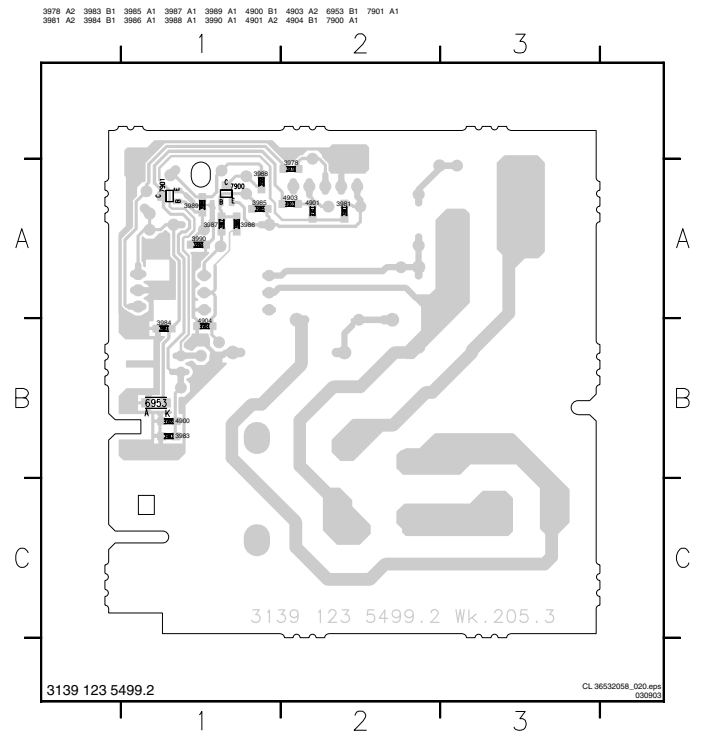
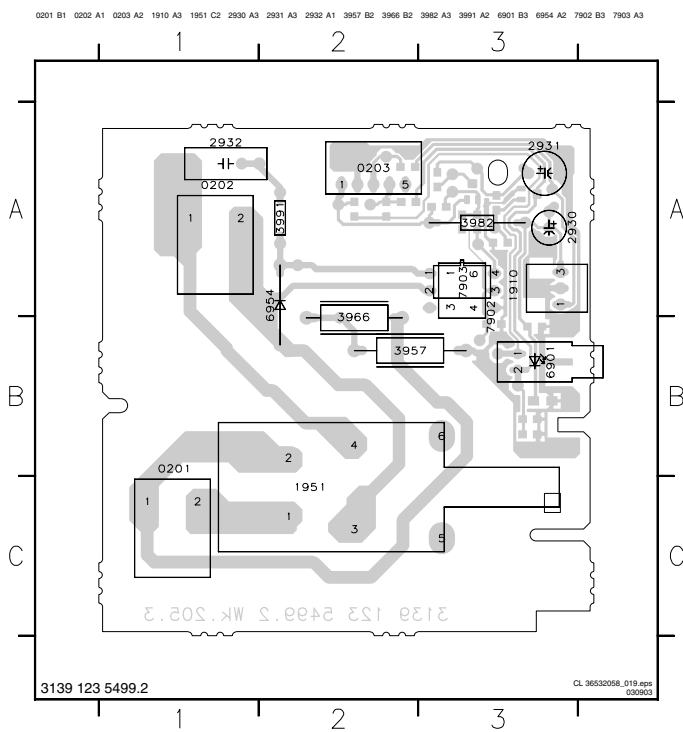


**J FRONT INTERFACE PANEL**



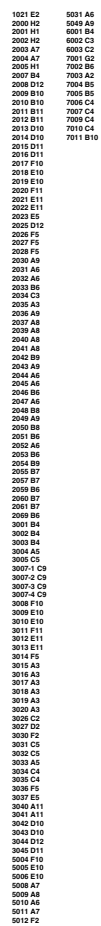
Layout Front Interface Panel PV2 Styling (Top Side)

Layout Front Interface Panel PV2 Styling (Bottom Side)

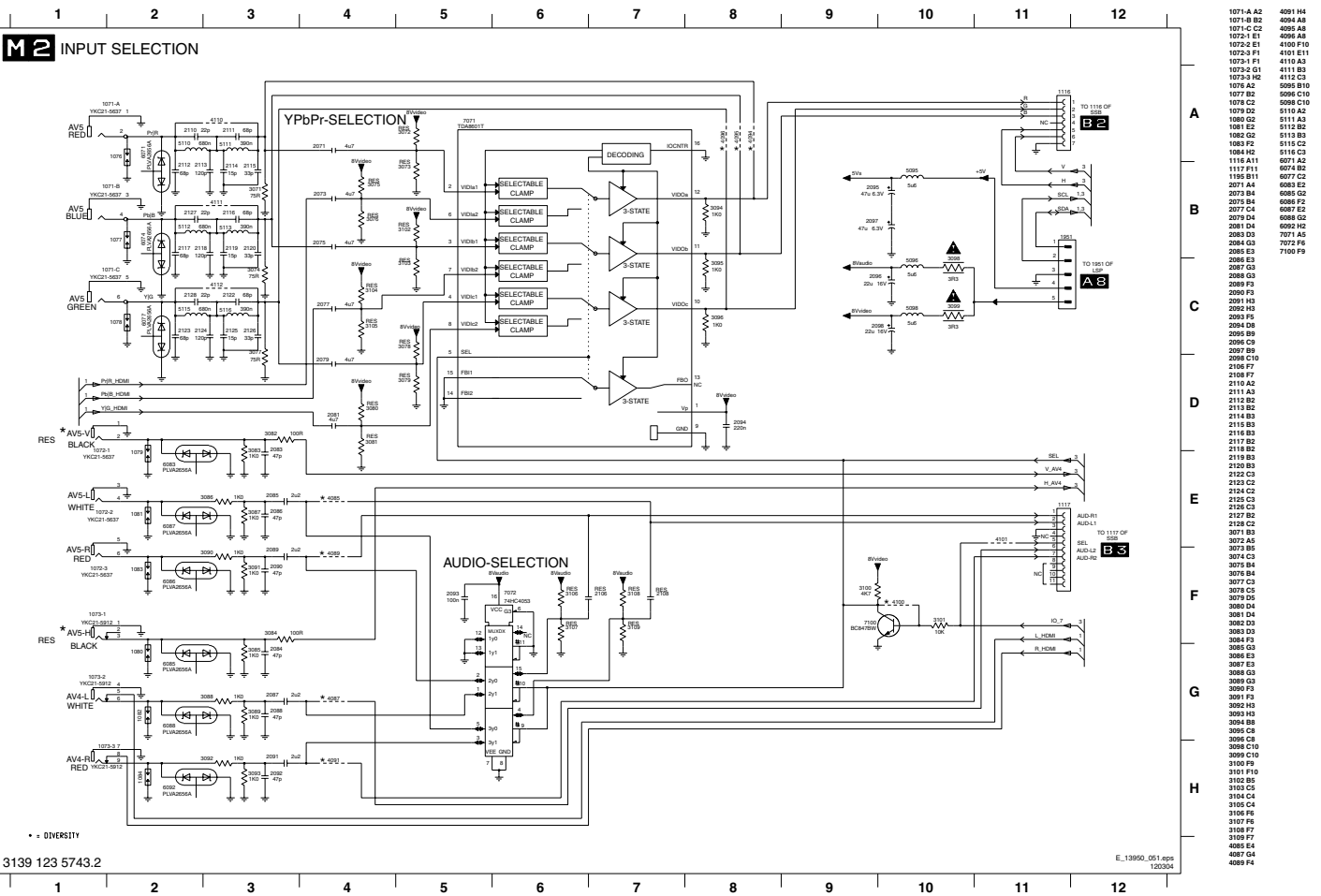




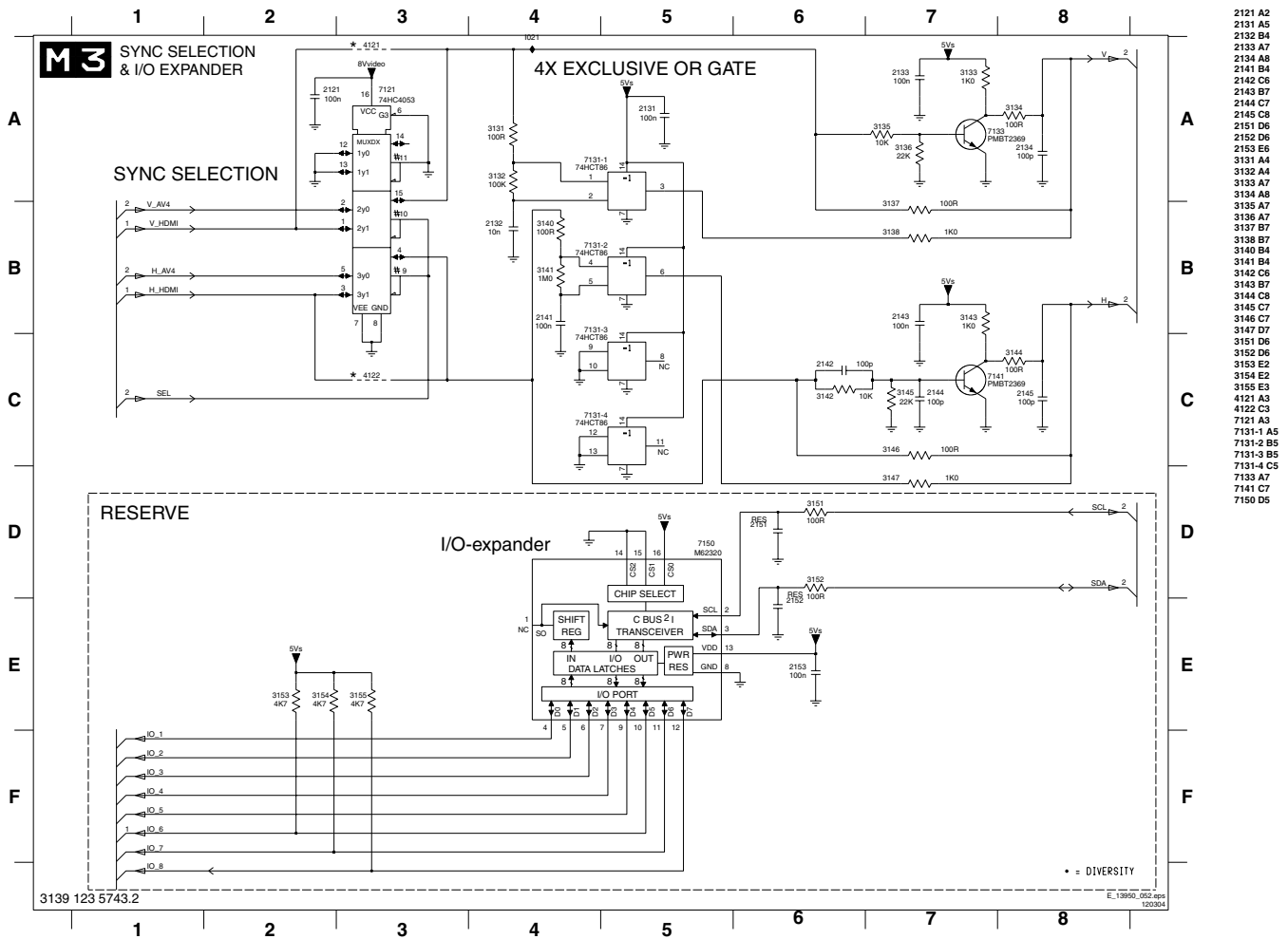
## M 1 HDMI PANELLINK RECEIVER



## HDMI Panel

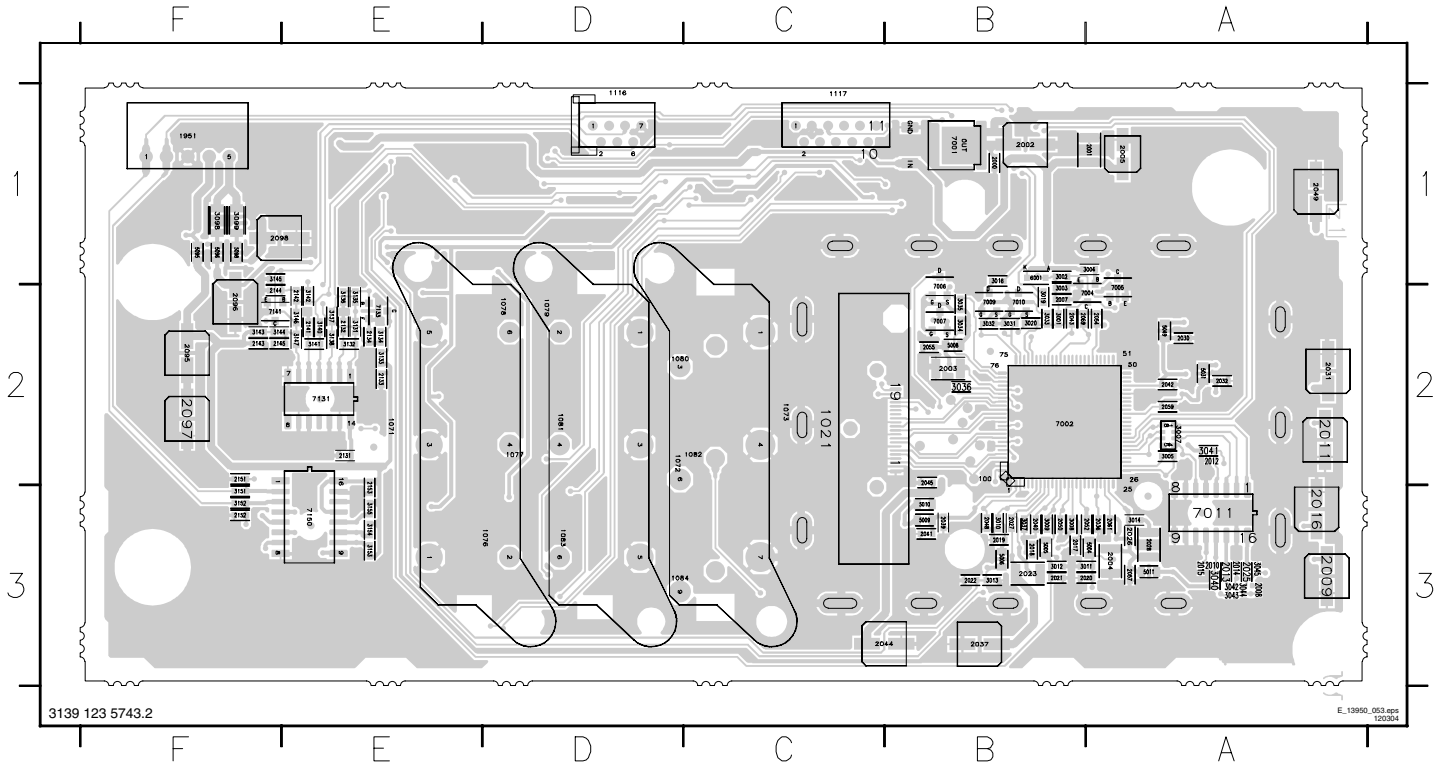


## HDMI Panel



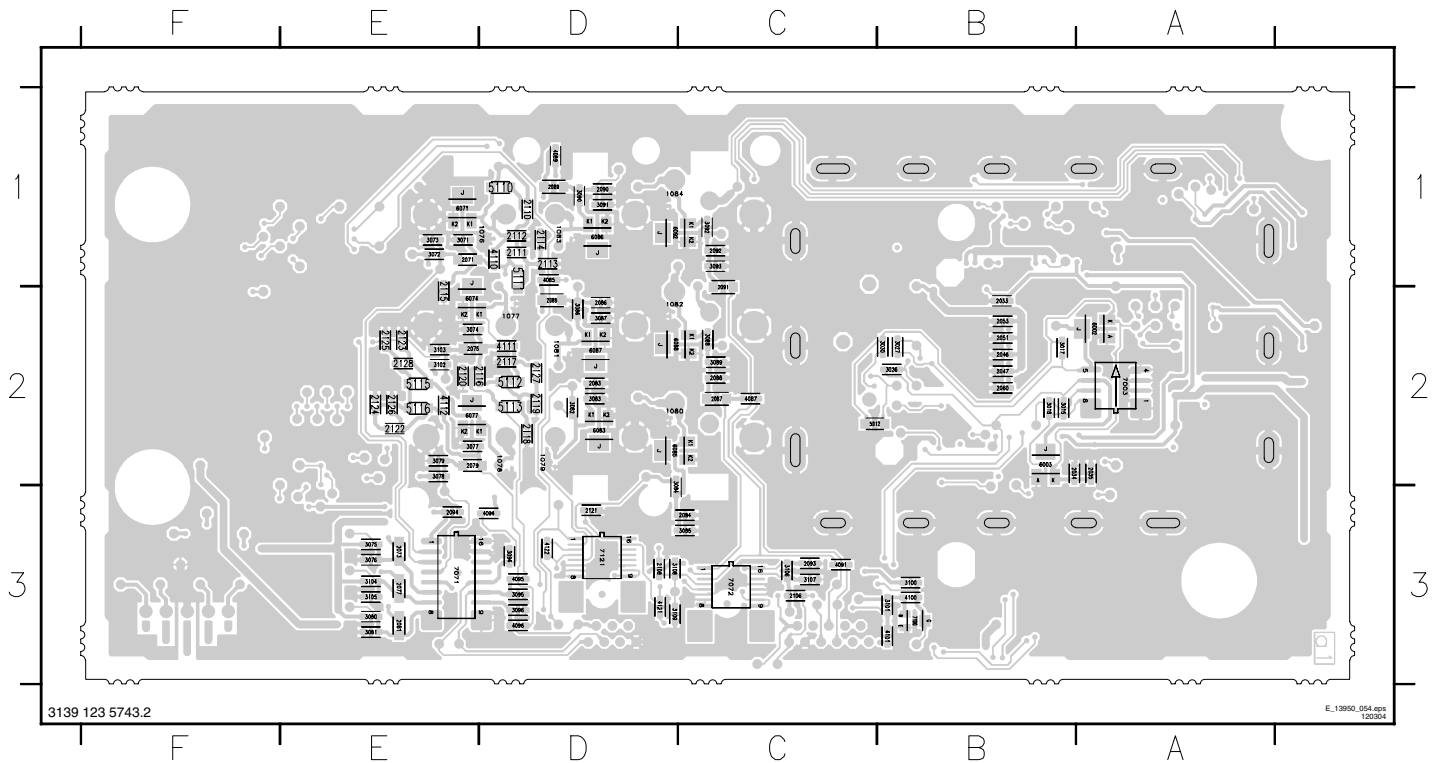
## Layout HDMI Panel (Top Side)

1021 C2	2007 B2	2020 A3	2039 B3	2057 A3	2142 E2	3008 B3	3034 B2	3132 E2	3146 E2	5011 A3	7009 B2
1071 E2	2008 A3	2021 B3	2040 B3	2059 A2	2143 F2	3009 B3	3035 B2	3133 E2	3147 E2	5031 A2	7010 B2
1072 D2	2009 A3	2022 B3	2041 B3	2061 A3	2144 F2	3010 B3	3036 B2	3134 E2	3151 F3	5049 A2	7011 A3
1073 C2	2010 A3	2023 B3	2042 A2	2069 B2	2145 F2	3011 A3	3037 B3	3135 E2	3152 F3	5095 F1	7131 E2
1116 D1	2011 A2	2025 A3	2043 B2	2096 F2	2151 F2	3012 B3	3040 A3	3136 E2	3153 E3	5096 F1	7133 E2
1117 C1	2012 A2	2026 A3	2044 C3	2098 F2	2152 F3	3013 B3	3041 A2	3137 E2	3154 E3	5098 F1	7141 F2
1951 F1	2013 A3	2027 B3	2045 B2	2097 F2	2153 E3	3014 A3	3042 A3	3138 E2	3155 E3	6001 B1	7150 E3
2000 B1	2014 A3	2028 A3	2048 B3	2098 F1	3001 B2	3016 B1	3043 A3	3140 E2	5004 A3	7001 B1	
2001 A1	2015 A3	2030 A2	2049 A1	2131 E2	3002 B1	3019 B2	3044 A3	3141 E2	5005 B3	7002 B2	
2002 B1	2016 A3	2031 A2	2050 B3	2132 E2	3003 B2	3020 B2	3045 A3	3142 E2	5006 B3	7004 A2	
2003 B2	2017 B3	2032 A2	2052 A3	2133 E2	3004 A1	3031 B2	3036 F1	3143 F2	5008 B2	7005 A2	
2004 A3	2018 B3	2036 A3	2054 A2	2134 E2	3005 A2	3032 B2	3099 F1	3144 F2	5009 B3	7006 B2	
2005 A1	2019 B3	2037 B3	2055 B2	2141 E2	3007 A2	3033 B2	3131 E2	3145 F1	5010 B3	7007 B2	

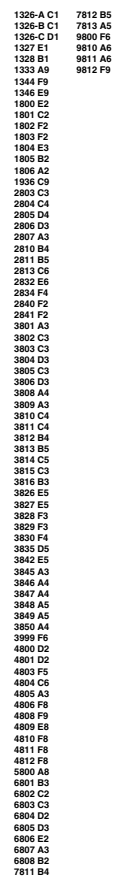


## Layout HDMI Panel (Bottom Side)

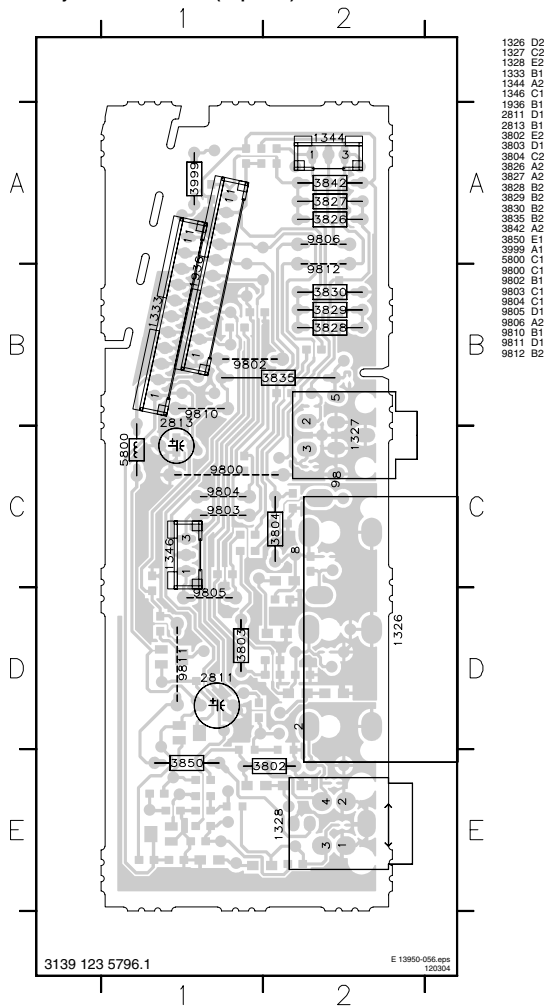
2033 B2	2079 E2	2093 C3	2118 D2	3017 B2	3078 E2	3090 D1	3105 E3	4100 B3	5115 E2	6092 D1
2034 B2	2081 E3	2094 E3	2119 D2	3018 B2	3079 E2	3091 D1	3106 C3	4101 B3	5116 E2	7003 A2
2035 A2	2083 D2	2106 C3	2120 E2	3026 B2	3080 E3	3092 C1	3107 C3	4110 D1	6002 A2	7071 E3
2046 B2	2084 C3	2108 D3	2121 D3	3027 B2	3081 E3	3093 C1	3108 D3	4111 D2	6003 B2	7072 C3
2047 B2	2085 D2	2110 D1	2122 E2	3030 B2	3082 D2	3094 D3	3109 D3	4112 E2	6071 E1	7100 B3
2051 B2	2086 D2	2111 D1	2123 E2	3071 E1	3083 D2	3095 D3	4085 D1	4121 D3	6074 E2	7121 D3
2053 B2	2087 C2	2112 D1	2124 E2	3072 E1	3084 D3	3096 D3	4087 C2	4122 D3	6077 E2	
2060 B2	2088 C2	2113 D1	2125 E2	3073 E1	3085 C3	3100 B3	4089 D1	5012 C2	6083 D2	
2071 E1	2089 D1	2114 D1	2126 E2	3074 E2	3086 D2	3101 B3	4091 C3	5110 D1	6085 D2	
2073 E3	2090 D1	2115 E2	2127 D2	3075 E3	3087 D2	3102 E2	4094 D3	5111 D1	6086 D1	
2075 E2	2091 C2	2116 D2	2128 E2	3076 E3	3088 C2	3103 E2	4095 D3	5112 D2	6087 D2	
2077 E3	2092 C1	2117 D2	3015 B2	3077 E2	3089 C2	3104 E3	4096 D3	5113 D2	6088 D2	



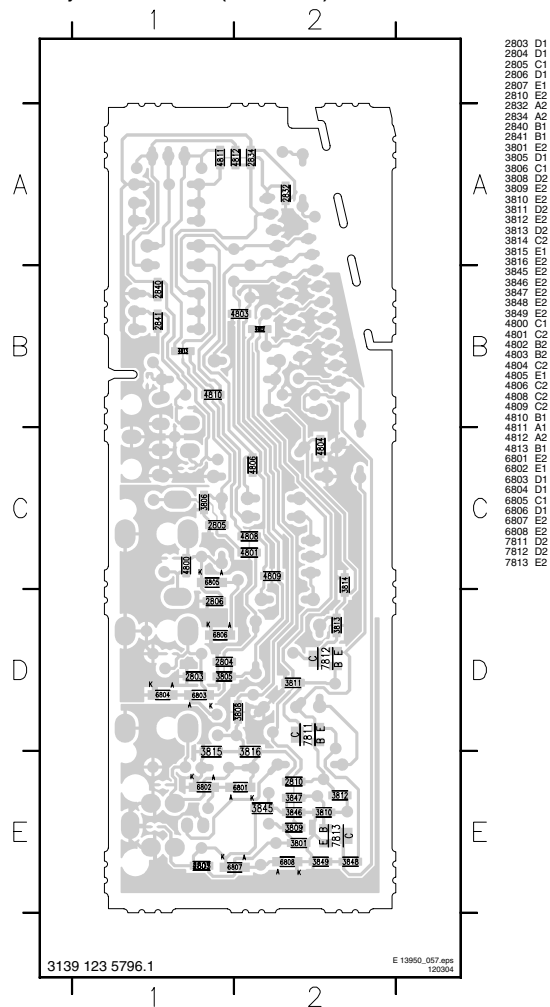
**SIDE I/O**



Layout Side I/O Panel (Top Side)



Layout Side I/O Panel (Bottom Side)

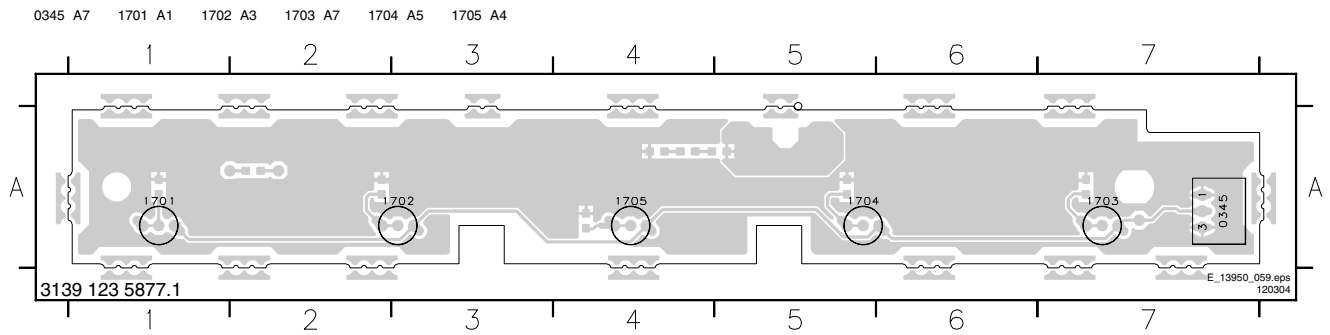
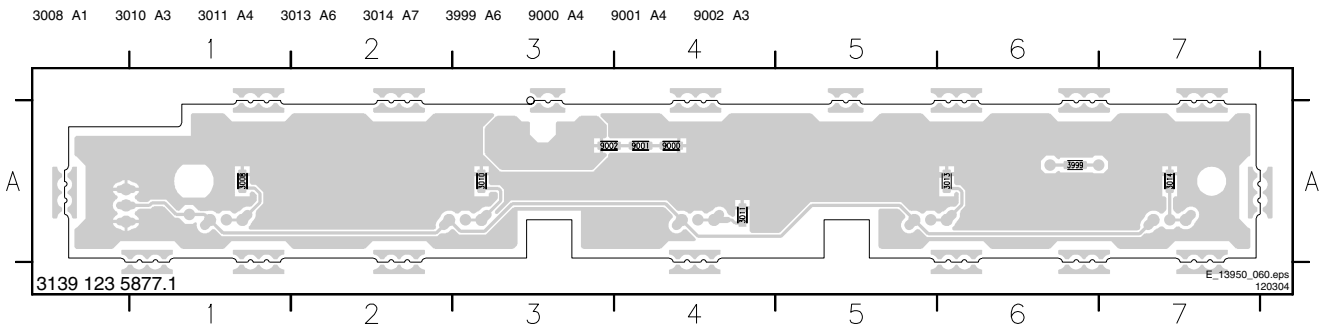


0345 A4	1703 A2	3008 B2	3013 B1	9000 C3
1701 A1	1704 A2	3010 B2	3014 B1	9001 C3
1702 A1	1705 A1	3011 B1	3999 C3	9002 C4



This image shows a single sheet of white paper with horizontal ruling lines. The lines are evenly spaced and run across the width of the page. There are no margins, text, or other markings on the paper.



**Layout Top Control Panel FL13 Styling (Top Side)****Layout Top Control Panel FL13 Styling (Bottom Side)**

1 2 3 4

# TOP CONTROL PANEL (PV2)

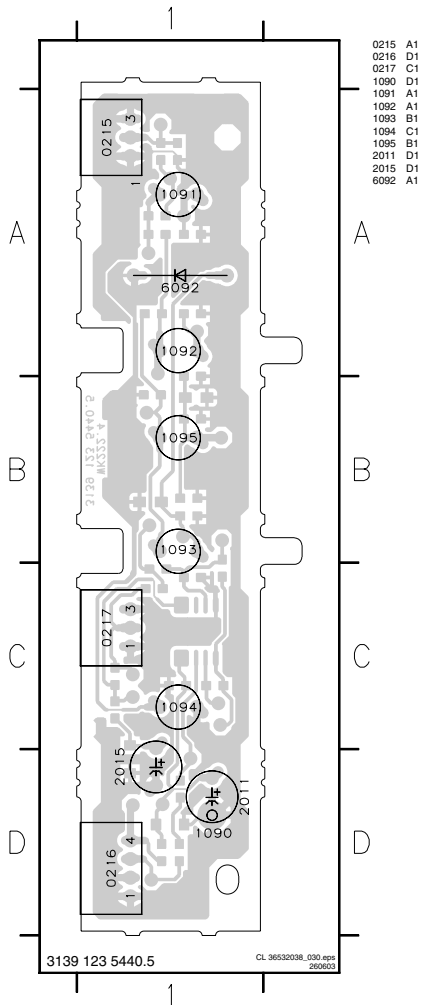
TO 1945  
OF  
FRONT  
(LSP)  
**A10**

**Personal Notes:**

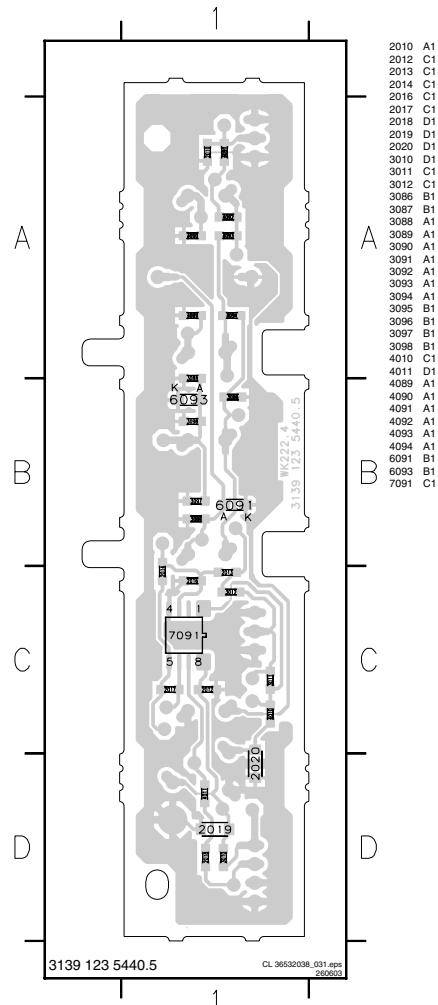
4 Keys	5 Keys	
2010	2010	4091
3091	3091	4092
3092	3092	4093
3093	3093	4094
3094	3094	3090
3095	3095	3089
3096	3096	3088
4090	3097	3087
4089	3098	3086
6090	4090	1091
1091	4089	1092
1092	6093	1093
1093	1091	1094
1094	1092	1095
	1093	
	1094	
	1095	

0215 A1  
1091 B2  
1092 B3  
1093 B4  
1094 B4  
1095 B3  
2010 A1  
3086 A4  
3087 B4  
3088 B3  
3089 B3  
3090 B2  
3091 A1  
3092 A2  
3093 A2  
3094 A3  
3095 A4  
3096 B4  
3097 B3  
3098 B3  
4089 B2  
4090 B2  
4091 A2  
4092 A2  
4093 A2  
4094 A3  
6091 B4  
6092 B4  
6093 B3

Layout Top Control Panel PV2 Styling (Top Side)



Layout Top Control Panel PV2 Styling (Bottom Side)



## This image shows a full page of blank, lined paper. It features approximately 20 evenly spaced horizontal grey lines across its entire width, providing a template for handwriting practice or general note-taking. The margins are consistent on all sides.

## 8. Alignments

Index of this chapter:

1. General alignment conditions
2. Hardware alignments
3. Software alignments
4. Option settings

### 8.1 General Alignment Conditions

#### 8.1.1 Default Alignment Settings

Perform all electrical adjustments under the following conditions:

- Power supply voltage: 120 V<sub>ac</sub> / 60 Hz (± 10 %).
- Connect the set to the mains via an isolation transformer with low internal resistance.
- Allow the set to warm up for approximately 20 to 30 minutes.
- Measure voltages and waveforms in relation to chassis ground (with the exception of the voltages on the primary side of the power supply). **Caution:** never use heatsinks as ground.
- Test probe: R<sub>i</sub> > 10 Mohm, C<sub>i</sub> < 20 pF.
- Use an isolated trimmer/screwdriver to perform alignments.

Perform all electrical adjustments with the following default settings (for all CRTs):

- Choose "Weak" picture mode with the (Smart) "Picture" button on the remote control.
- Set "Dynamic Contrast" (accessible via MENU -> PICTURE) and "Active Control" (on remote control) to "off" (if either one of them is present).
- Set "Brightness" (accessible via MENU -> PICTURE) to aligned value unless otherwise specified.

#### 8.1.2 Adjustment Sequence

Use the following adjustment sequence:

1. Set the correct TV-set OPTIONS as described in paragraph "Options". After storing, re-start the set.
2. Rough adjustment of VG2 and FOCUS.
3. RF-AGC alignment.
4. IF-PLL OFFSET adjustment.
5. Rough adjustment of GEOMETRY.
6. Allow the set to warm up.
7. Precise adjustment of VG2 and FOCUS.
8. Precise adjustment of GEOMETRY.
9. PIP alignments (if present).
10. COLOR alignments.
11. Other software alignments.

### 8.2 Hardware Alignments

#### Notes:

- The Service Alignment Mode (SAM) is described in chapter 5 "Service Modes, Error Codes, and Fault Finding".
- Use the cursor-, menu-, and OK-buttons of the remote control (RC) transmitter for navigation.

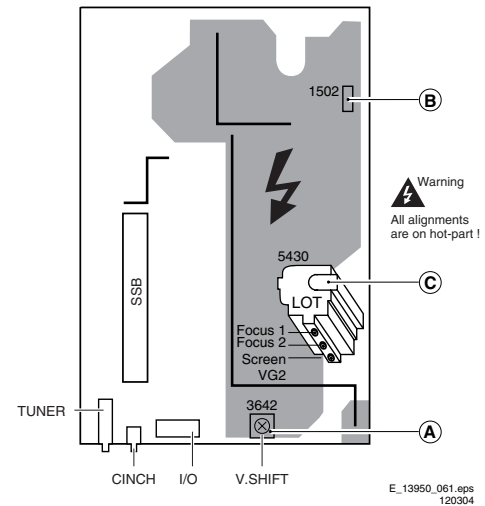


Figure 8-1 Top view LSP

#### 8.2.1 Vg2 Adjustment

##### Notes:

- For adjusting the Vg2 in A10 sets, the vertical scan had to be disabled by the VSD bit (Vertical Scan Disable). However, do **not** use this option in this chassis (when present, because not used in all software), as it will lead to a "beam current" protection!
- Also, the option "VG2" in the SAM does not function yet. Please, do **not** use!

In the frame-blanking period of the R, G, and B signals applied to the CRT, the video processor inserts a measuring pulse with different DC levels. Measure the black level pulse during the vertical flyback at the RGB cathodes of the CRT.

1. Connect the RF output of a pattern generator to the antenna input. Input a "black" picture (blank screen on CRT without any OSD info) test pattern.
2. Use the MENU key to enter the "user" menu, select "Picture", and set "Brightness" and "Contrast" to minimum (write down the original settings).
3. Set the oscilloscope to 20 V/div and the time base to 20 us/div. Use external triggering on the vertical pulse (**caution:** use a trigger point on the "cold" side!)
4. Ground the scope on the CRT panel ("cold" side) and connect a 10:1 probe to one of the cathodes of the picture tube socket (see circuit diagram F).
5. Measure at test points F017, F018 and F019 on the picture tube socket (or pins 6, 8, and 11) the DC-level of the measuring pulse (1st full line after the frame blanking) with respect to earth.
6. Select the pin with the highest level found and adjust V<sub>cutoff</sub> by means of the Vg2-potmeter (lowest-one) on the Line Output Transformer (LOT) to 165 ± 5 V<sub>dc</sub> (for all screen sizes).
7. Reset "Contrast" and "Brightness" to their original values (as written down).

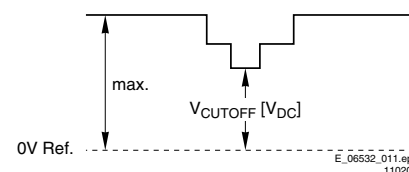


Figure 8-2 Waveform Vg2 alignment

### 8.2.2 Focus alignment

The LOT has the following outline:

- Focus 1 (F1)= Static alignment (black wire).
  - Focus 2 (F2)= Dynamic alignment (red wire).
1. Use an external video pattern generator to input a "circle" or "crosshatch" test pattern to the set.
  2. Choose "Weak" picture mode with the (Smart) "Picture" button on the remote control transmitter.
  3. Adjust the "dynamic focus 2" potentiometer (in the middle on the LOT) until the horizontal lines at the centre of the screen are of minimum width without introducing a visible haze.
  4. Adjust the "static focus 1" potentiometer (highest of the LOT) until the horizontal lines at the sides of the screen are of minimum width without introducing a visible haze.
  5. Repeat these two steps to achieve the best result.

## 8.3 Software Alignments

Put the set in the SAM (see the "Service Modes, Error Codes and Fault Finding" section). The SAM menu will now appear on the screen. The different alignment parameters are described further on.

### Notes:

- All changes to menu items and alignments must be stored manually.
- If an empty EARAM (permanent memory) is detected, all settings are set to pre-programmed default values, so the set must be re-aligned.

### 8.3.1 TUNER

#### IF PLL OFFSET

No adjustments needed: default value is "35".

If the mentioned default value does not give the required result, use the following alignment method:

1. Set an external pattern generator to a crosshatch video signal and connect the RF output to the aerial input of the TV. Set the amplitude to 10 mV and the frequency to 61.25 MHz. Use system NTSC M if possible, otherwise match the system of your generator with the received signal in the set.
  - For "Negative modulation", the **sound** signal must be a non-modulated FM signal.
  - For "Positive modulation", the **video** signal must have high modulation (100% or above).
2. Put the set in the SAM mode.
3. Select via the TUNER menu, the IF-PLL OFFSET sub-menu.
4. Measure and align:
  - For "Negative modulation", on MONITOR OUT (**audio**): Adjust IF-PLL OFFSET until the largest Signal Noise Ratio (SNR) is reached.
  - For "Positive modulation", on MONITOR OUT (**video**): Adjust IF-PLL OFFSET until you get minimal V-sync disturbance.

#### AGC

1. Set an external pattern generator to a color bar video signal and connect the RF output to the aerial input of the TV. Set the amplitude to 10 mV and the frequency to 61.25 MHz. Use system NTSC M if possible, otherwise match the system of your generator with the received signal in the set.
2. Put the set in the SAM mode.
3. Select via the TUNER menu, the AGC sub-menu.
4. Connect a DC multi-meter to pin 1 of the tuner (item 1200 on the LSP).
5. Adjust the AGC until the voltage at pin 1 of the tuner is 3.3 V (+/- 0.1 V). The value can be incremented or

decremented by pressing the right/left CURSOR button on the RC.

6. After alignment, save the value(s) with the STORE command in the SAM main menu.

#### 2nd AGC

Same alignment as AGC-alignment however for a second tuner (when applicable, e.g. PIP or DW).

### 8.3.2 WHITE TONE

In the WHITE TONE sub menu, the color values for the different color temperatures can be aligned.

The color temperature mode (NORMAL, DELTA COOL, DELTA WARM) can be selected per color (R, G, and B) with the RIGHT/LEFT cursor keys. The mode or value can be changed with the UP/DOWN cursor keys.

First, the values for the NORMAL color temperature must be aligned. Then the offset values for the DELTA COOL and DELTA WARM mode can be aligned. Note that the alignment values are non-linear.

#### Alignment

No adjustments needed. Use the given default values:

Table 8-1 White tone alignment (default values)

Parameter	27PT8302/37	32PT8302/37	30PW8402/37	34PW8402/37
Normal Red	10	0	0	0
Normal Green	3	-8	-7	-8
Normal Blue	2	1	-6	1
Red BL Offset	7	7	7	7
Green BL Offset	7	7	7	7
Blue BL Offset	7	7	7	7
Delta Cool Red	0	0	0	0
Delta Cool Green	2	3	2	2
Delta Cool Blue	11	12	12	10
Delta Warm Red	0	0	0	0
Delta Warm Green	-7	-6	-8	-7
Delta Warm Blue	-22	-20	-24	-21

If the mentioned default values do not give the required result, use the following alignment method:

1. Set the external pattern generator to a 100% white pattern, and connect the RF output to the aerial input of the TV. Set the amplitude at least 1 mV<sub>rms</sub> (60 dBuV) and the frequency to 61.25 MHz. Use system NTSC M if possible, otherwise match the system of your generator with the received signal in the set.
2. Set "Smart Picture" to "Weak".
3. Set "Dynamic NR" to "off" (accessible via MENU -> Features).
4. Put the set in the SAM mode.
5. Set NORMAL GREEN to "32".
6. Measure with the color analyzer (Minolta CA100 Color Analyzer or equivalent), calibrated with the spectra, on the centre of the screen.
7. Adjust with the cursor left/right command the Red and Blue register for the right xy-coordinates (see next table).
8. Repeat the white tone adjustment also for the color temperatures COOL and WARM.

Table 8-2 White tone alignment (with color analyzer)

White D mode	Temperature	DUV	x	y
Normal	9300 K	+0.003	282 +/- 8	298 +/- 8
Cool	12000 K	+0.003	270 +/- 8	280 +/- 8
Warm	6500 K	+0.003	315 +/- 8	325 +/- 8

## 8.3.3 GEOMETRY

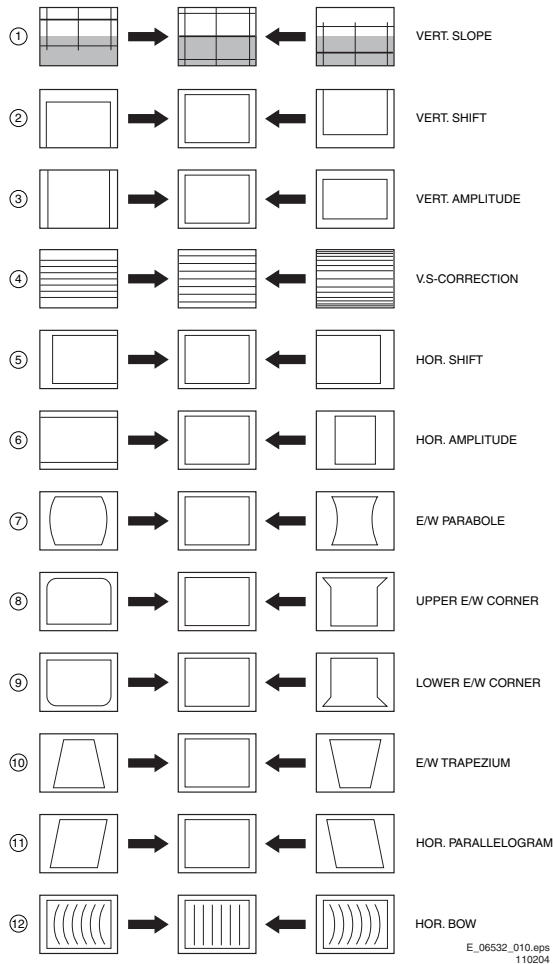


Figure 8-3 Geometry Alignments

**Notes:**

- Set an **external** pattern generator to a crosshatch video signal and connect the RF output to the aerial input of the TV. Set the amplitude at least 1 mV<sub>rms</sub> (60 dBuV) and the frequency to 61.25 MHz. Use system NTSC M if possible, otherwise match the system of your generator with the received signal in the set.  
**Note:** Do **not** use the internal test pattern from the GEOMETRY menu!
- Use the default alignment settings, but set "Brightness" to "32".
- For wide screen models, set to "wide screen" mode, for "classic" models, set to "4:3".
- After alignment, save the value(s) with the STORE command in the SAM main menu.

**Service tip:** When the set is equipped with a rotation coil, use this menu item to check its correct alignment. If alignment is not correct, go to the user MENU, choose FEATURES, and select ROTATION. With the use of a crosshatch test pattern, align it to a correct horizontal picture.

**Alignment**

No adjustments needed. Use the given default values:

Table 8-3 Geometry alignment (default values)

Item	27PT8302/37	32PT8302/37	30PW8402/37	34PW8402/37
VERT.SHIFT	0	0	0	0
VER.AMPL	-17	8	-15	-8
VER.SCOR	19	12	6	6
VER.U_LIN	0	-3	0	0
VER.L_LIN	0	17	0	0
HOR.SHIFT	-54	-69	50	-42
EW.WIDTH	-55	-93	45	-40
EW_1	-85	-100	-73	-80
EW_2	-54	-54	-37	-45
EW_3	-31	-10	-19	-25
EW_4	-10	30	-6	-9
EW_5	0	50	0	0
EW_6	0	50	0	0
EW_7	-7	35	-7	-7
EW_8	-27	-1	-22	-24
EW_9	-51	-52	-41	-49
EW_10	-76	-110	-76	-64
HOR.BOW	0	4	2	3
HOR.PARALLEL	0	1	2	1
HOR.LIN	0	-12	0	0
HOR.SCOR	0	0	0	0
HOR.IN_PIN	0	0	0	0

If the mentioned default values do not give the required result, use the following alignment method:

- Before starting the vertical alignment, set (in SAM) the following parameters to "0":
  - VER. SHIFT,
  - VER. SCOR,
  - VER. U\_LIN,
  - VER. L\_LIN.
- Set SERV. BLK to "on", to blank the lower half of the screen.
- Adjust the "VERTICAL SHIFT" potentiometer (R3642 on the LSP) until the picture is centered (to the mechanical centre of the picture tube), and switch SERV. BLK to "off".
- Adjust VER. U\_LIN and VER. L\_LIN such, that upper and lower horizontal lines of the crosshatch pattern are just visible.

Use then the following software regulations to modify the geometry:

- VER. AMPL (Vertical Amplitude): Align for the vertical picture centre, range from -32 to +32.
- VER. SHIFT (Vertical Shift): Compensating for any gain error in amplifier, adjust range from -32 to +32 to the proper amplitude.
- VER. SCOR (Vertical S-Correction): Align for equal height of the blocks in the top, the bottom and the middle, range from -63 to +63.
- HOR. SHIFT (Horizontal Shift): Adjust for the horizontal centre of the screen, range from -127 to +128.

Next step is to align the East/West geometry.

- First, set the parameters EW\_5 and EW\_6 to "0"
- EW. WIDTH (East-West Width): This sets the (overall) horizontal size of the picture on the screen. Range from -63 to +63 (with the following EW alignments, these lines can be straightened).

3. EW\_1 (East-West parameter 1): Has effect on the length of the upper part of the vertical E/W lines.
4. EW\_2 (East-West parameter 2): Has effect on the length of the vertical E/W lines just below EW\_1.
5. EW\_3 (East-West parameter 3): Has effect on the length of the vertical E/W lines just below EW\_2.
6. EW\_4 (East-West parameter 4): Has effect on the length of the vertical E/W lines just below EW\_3.
7. EW\_5 (East-West parameter 5): Has effect on the length of the vertical E/W lines just below EW\_4.
8. EW\_6 (East-West parameter 6): Has effect on the length of the vertical E/W lines just below EW\_5.
9. EW\_7 (East-West parameter 7): Has effect on the length of the vertical E/W lines just below EW\_6.
10. EW\_8 (East-West parameter 8): Has effect on the length of the vertical E/W lines just below EW\_7.
11. EW\_9 (East-West parameter 9): Has effect on the length of the vertical E/W lines just below EW\_8.
12. EW\_10 (East-West parameters 10): Has effect on the length of the lowest part of the vertical E/W lines.
13. HOR. BOW (Horizontal Bow): Align the EW parabola to be symmetrical, range from -63 to +63.
14. HOR. PARALLEL (Horizontal Parallel): Align for straight vertical lines on the picture sides, range from -63 to +63.
15. HOR. LIN (Horizontal Linearity): Align for equal width of horizontal blocks on the left, the right and the centre, range from 0 to +127.
16. HOR. IN\_PIN (Horizontal Inner Pincushion): Align for the inner straight vertical lines, range from 0 to +32.

### 8.3.4 SOUND

No adjustments needed. Use the given default values:

- PRESCALE LEVEL
  - FM: "+1".
  - EXTAM Gain: "0".
  - PIPMONO: "0".
  - ExtLR-in: "0".
  - SAP: "0".
- TRESHOLD LEVEL
  - Over Mod Tresh: "+3dB".
  - NoiseTres SC2: "+2".
  - NoiseHyst SC2: "+4".
  - NoiseTres SAP: "+4".
  - NoiseHyst SAP: "0".
  - Nmute BTSC Hyst: "+7".
  - Nmute BTSC Thr: "+4".
- EFFECTS LEVEL
  - BMT CutOffFrq: "50Hz".
  - Incredible SND: "60%".
  - VDolby: "100%".

### 8.3.5 SMART SETTINGS

No adjustments needed. Use the given default values (differs per selected source):

**Table 8-4 Smart settings (default values)**

Smart setting		RF-source	AV-source (480i, 480p)	HD-source (1080i)
MOVIES	BGT	42	42	40
	COL	46	46	46
	CON	60	55	65
	SHP	3	3	3
	HUE	52	52	46
SPORTS	BGT	51	46	44
	COL	50	50	48
	CON	90	85	90
	SHP	5	5	5
	HUE	52	52	46
WEAK	BGT	46	44	42
	COL	46	46	46
	CON	75	70	75
	SHP	1	1	1
	HUE	52	52	46
MULTI	BGT	51	48	46
	COL	55	55	50
	CON	95	90	95
	SHP	6	6	6
	HUE	52	52	46

BGT= Brightness, COL= Color, CON= Contrast, SHP= Sharpness, HUE= Hue.

## 8.4 OPTIONS

### 8.4.1 Introduction

The microprocessor communicates with a large number of I2C ICs in the set. To ensure good communication and to make digital diagnosis possible, the microprocessor has to know which ICs to address. The presence / absence of these specific ICs (or functions) is made known by the option codes.

#### Notes:

- After changing the option(s), leave the OPTIONS submenu, and save them with the STORE command.
- The set must be disconnected from AC power to change and store the option codes. If the television is only turned "off" with the Power switch, the option code settings are NOT read by the microprocessor.
- When the EARAM is replaced, all options will require resetting. To be certain that the factory settings are reproduced exactly, you must set all option number lines. Normally, you can find the correct option numbers on the CRT sticker inside the TV set. If the CRT sticker is damaged or not present, you can use the options listed in the option code table below.

**Example:** The CRT sticker (or SAM menu) shows the following option numbers:

- OB1= 8331
- OB2= 225
- OB3= 913
- Etc.

Every number represents 16 bits (so the maximum number will be 65536 if all options are set to on).



When all the correct options are set, the sum of the decimal values of each Option Byte (OB) will give the option number.

#### 8.4.2 Changing options

Options are used to control the presence / absence of certain features and hardware. There are two ways to change the option settings, which are explained below. Selecting STORE and pressing the CURSOR RIGHT key save all changes in the option settings. Some changes will only take affect after the set has been switched "off" and "on" with the mains switch (cold start).

##### **Changing multiple options by changing option byte values**

An option number (or "option byte") represents a number of different options. When you change these numbers directly, you can set all options very quickly. All options are controlled via these option numbers.

- To change the option numbers, select the Option Byte you want to change with the CURSOR UP/DOWN keys, and key in the new value. See table "Option bit overview" for more details. An explanation per option is listed in paragraph "Option Bit Definition".
- Changes to the option codes must be stored manually.

**Table 8-5 Option byte settings**

Option Byte	27PT8302/37	32PT8302/37	30PW8402/37	34PW8402/37
OB1	8331	8331	24715	24715
OB2	225	225	225	225
OB3	657	657	913	913
OB4	129	129	129	129
OB5	64	64	64	64
OB6	20480	20480	20480	20480
OB7	6720	6720	6720	6720
OB8	5	261	261	261
OB9	24017	24017	24017	24017
OB10	793	795	2843	2843
OB11	7309	7309	7309	7309
OB12	11008	11008	11008	11008
OB13	704	704	704	704

##### **Changing a single option**

It is also possible to change an option one at a time. Therefore, select the option with the CURSOR UP/DOWN keys and change its setting with the LEFT/RIGHT keys.

**Table 8-6 Option bit settings**

Option Bit	30PW8402/37	34PW8402/37	32PT8302/37	27PT8302/37
2CVI	On	On	On	On
HDMI	On	On	On	On
ASPR	On	On	Off	Off
EXCF	Off	Off	Off	Off
DCMU	On	On	On	On
HIST	On	On	On	On
DCMU	On	On	On	On
DNR	On	On	On	On
BBD	Off	Off	Off	Off
HDSF	Off	Off	Off	Off
CZOM	Off	Off	Off	Off
HSHT	On	On	Off	Off
SSHT	On	On	Off	Off
APC	On	On	On	On
ROTI	On	On	On	On
ISMU	On	On	On	On
AAVL	On	On	On	On
SPKC	On	On	On	On
DBYV	On	On	On	On
EQTO	Off	Off	Off	Off
BASF	DBE	DBE	DBE	DBE
AOUT	On	On	On	On
HPMN	Off	Off	Off	Off
QPEAK	Off	Off	Off	Off
PITN	Off	Off	Off	Off
FUNN	Off	Off	Off	Off
USTN	On	On	On	On
SURF	On	On	On	On
SZAP	On	On	On	On
PLST	On	On	On	On
PIPC	Off	Off	Off	Off
PIPT	Off	Off	Off	Off
W4X3	Off	Off	Off	Off
W169	Off	Off	Off	Off
SMCK	On	On	On	On
TIME	On	On	On	On
CCAP	On	On	On	On
VCBK	On	On	On	On
VBNR	On	On	On	On
SOSD	On	On	On	On
BNUM	On	On	On	On
STOR	Off	Off	Off	Off
SBNP	On	On	On	On
AUSB	On	On	On	On
HOSP	Off	Off	Off	Off

### 8.4.3 Option Bit Definition

**Note:** This chassis is global. Therefore **all** available options are listed below. It depends on the region which options are used in the set.

#### Sources

**CVI:** AV1 CVI source.

Function: Disabled/Enabled AV1 CVI source.

Values: OFF= Disabled, AV1 CVI source is not available. ON= Enabled, AV1 CVI source is available.

**AV3:** Side AV source.

Function: Disabled/Enabled side AV source.

Values: OFF= Disabled, side AV source is not available. ON= Enabled, side AV source is available.

**SCT3:** SCART 3 input.

Function: Disabled/Enabled SCART3 input.

Values: OFF= Disabled. ON= Enabled.

**VGA:** 2FH VGA input.

Function: Disabled/Enabled 2FH VGA input.

Values: OFF= Disabled. ON= Enabled.

**2CVI:** 2FH CVI input.

Function: Disabled/Enabled 2FH CVI input.

Values: OFF= Disabled. ON= Enabled.

**HDMI:** HDMI input.

Function: Disabled/Enabled HDMI input.

Values: OFF= Disabled. ON= Enabled.

#### Video

**ASPR:** Aspect Ratio Setting.

Function: Select between 4 by 3 or 16 by 9 set.

Values: OFF= 4 by 3 set. ON= 16 by 9 set.

**VMUT:** Video Mute.

Function: Disabled/Enabled video mute (blanking) during channel change.

Values: OFF= Disabled. ON= Enabled.

**EXCF:** External Comb Filter.

Function: To determine the availability of 3D comb filter on the SSB.

Values: OFF= Disabled, the 3D comb filter is not available.

ON= Enabled, the 3D comb filter is available.

**DCMU:** Dynamic Contrast via Menu.

Function: Disabled/Enabled Dynamic Contrast menu item.

Values: OFF= Disabled, Dynamic Contrast menu item is not available. ON= Enabled, Dynamic Contrast menu item is available.

Note: Dynamic Contrast via RC should always work (for all region).

**DNR:** Dynamic Noise Reduction.

Function: Disable/Enable (Dynamic) Noise Reduction function.

Values: OFF=Disabled. ON= Enabled.

**BBD:** Black Bar Detection.

Function: Disable/Enable Black Bar Detection.

Values: OFF=Disabled, Black Bar Detection not available. ON= Enabled, Black Bar Detection available.

Note: The Auto Screen Fit will not be included in the picture size loop when BBD is OFF.

**ASF:** Auto Screen Fit.

Function: Disable/Enable Auto Screen Fit.

Values: OFF=Disabled, Auto Screen Fit is not available. ON= Enabled, Auto Screen is Fit available.

Note: This option is only applicable to A02E 2003 (EU Basic).

**HDSF:** High Definition Screen Fit.

Function: Disabled/Enabled High Definition Screen Fit.

Values: OFF=Disabled, High Definition Screen Fit is not available. ON= Enabled, High Definition Screen is Fit available.

**CZOM:** Continuous Zoom.

Function: Disable/Enable Continuous Zoom.

Values: OFF=Disabled. ON= Enabled.

**HSHT:** Heading Shift.

Function: Disable/Enable Heading Shift.

Values: OFF=Disabled. ON= Enabled.

**SSHT:** Subtitle Shift.

Function: Disable/Enable Subtitle Shift.

Values: OFF=Disabled. ON= Enabled.

**APC:** Auto Picture Control (Auto TV).

Function: Disable/Enable Auto picture control.

Values: OFF= Disabled. ON= Enabled.

**WSSB:** Wide Screen Signaling Bit.

Function: Disable/Enable Wide screen Signaling bit function.

Values: OFF= Disabled. ON= Enabled.

**ROTI:** Rotation Tilt.

Function: Change the tilt level of picture tube.

Values: OFF= Disabled, menu item ROTATION is not available. ON= Enabled, menu item ROTATION is available.

**DGSC:** Digital Scan.

Function: Enable/Disable the Digital Scan in the DIGITAL OPT menu.

Values: OFF= Disabled, menu item DIG SCAN is not available. ON= Enabled, menu item DIG SCAN is available.

**SCAVM:** SCAVEM.

Function: Enable/Disable SCAVEM.

Values: OFF= Disabled. ON= Enabled.

#### Audio

**ISMU:** Incredible Surround through Menu.

Function: Disabled/Enabled incredible stereo (through Menu) function.

Values: OFF= Disabled, menu item INCREDIBLE STEREO (through Menu) is not available. ON= Enabled, menu item INCREDIBLE STEREO (through Menu) available.

**AAVL:** Automatic Volume Level control.

Function: Disable/Enable automatic volume leveler function.

Values: OFF=Disabled, menu item AVL is not available. ON= Enabled, menu item AVL is available.

**SPKC:** Speaker Control.

Function: Disabled/Enabled internal speakers.

Values: OFF= Disabled, menu item SPEAKERS is not available. ON= Enabled, menu item SPEAKERS is available. Note: SPEAKERS menu item is present in SOUND submenu when SPKC is ON.

**DBYV:** Dolby Virtual.

Function: Select surround setting.

Values: OFF= Disabled, DOLBY VIRTUAL setting is not available. ON= Enabled, DOLBY VIRTUAL setting is available. Note: Incredible surround & Dolby virtual are mutually exclusive.

**EQTO:** Equalizer or Tone control.

Function: Selection between Equalizer and Tone control (Bass and Treble).

Values: OFF= Tone control (Bass and Treble). ON= Equalizer. Note: Equalizer and Tone (Bass and treble) control are mutually exclusive.

**BASF:** Bass Feature.

Function: Select Dynamic (DBE) and Ultra Bass (DUB).

Values: 00= Disable DBE and DUB, 01= Enable DBE, 10= Enable DUB, 11= Not used.

**AOUT:** Audio Out.

Function: Disable/Enable menu item AUDIO OUT.

Values: OFF= Disabled, menu item AUDIO OUT is not available. ON= Enabled, menu item AUDIO OUT is available.

**HPMN:** Headphone Menu.

Function: Disable/Enable headphone menu.

Values: OFF= Disabled, Headphone submenu is not available. ON= Enabled, Headphone submenu is available.

**QPEAK:** AV Sound Mode detection.

Function: The current Sound Mode detection in AV is not working correctly. The optimal threshold value for the correct sound mode detection is still being investigated. Therefore, this is needed to disable the Sound Mode detection in AV until the correct threshold is identified.

Value: OFF= Disabled, AV sound auto detection is not available. ON= Enabled. AV sound auto detection is available.

**SWOF:** Subwoofer Selection.

Function: Disabled/Enabled Subwoofer.

Values: 00= Disabled, Subwoofer not available, 01= Enabled, Subwoofer is available, 10= Not Used, 11= Not used.

Note: This option is only for AP.

**Tuning**

**PITN:** Philips Tuner.

Function: Choose the tuner type that is configured in the hardware.

Values: 00= Disabled, ALPS compatible tuner is used. 01= Enabled, Philips compatible tuner is used, 10= Not Used, 11= Not Used.

**CHNA:** China.

Function: Set China Tuning IF Frequency.

Values: OFF= Disabled, Tuning is not for China TV set, ON= Enabled, Tuning is for China TV set.

Note: This option is also used to differentiate the AP China and AP Multi clusters. If CHNA is set to OFF, it is referring to AP Multi. If CHNA is ON, it is referring to AP China.

**FUNN:** Fine Tuning.

Function: Disabled/Enabled submenu, which allows fine-tuning of channel and storing the adjusted value.

Values: OFF= Disabled, menu item MANUAL is not available. ON= Enabled, menu item MANUAL is available

**USTN:** USA Tuning.

Function: Disabled/Enabled USA Tuning.

Values: OFF= Disabled. ON= Enabled.

**Installation**

**ACI:** Automatic Channel Installation.

Function: Disable/Enable automatic channel installation.

Values: OFF= Disabled Automatic Channel Installation. ON= Enabled Automatic Channel Installation.

Note: Download present program when ACI is ON.

**ATS:** Automatic Tuning System.

Function: Disable/Enable automatic tuning system.

Values: OFF= Disabled, automatic tuning system is ignored. ON= Enabled Automatic Tuning System, sort the program in an ascending order starting from Program 1.

Note: Sort the program in an ascending order starting from Program 1 when ATS is ON.

**MALY:** Malay Language.

Function: Disabled/Enabled Malay Language.

Values: OFF= Disabled. ON= Enabled.

**VMOD:** Virgin Mode.

Function: Disable/Enable virgin mode.

Values: OFF= Disabled, cannot access virgin mode. ON= Enabled, can access virgin mode.

Note: Plug and Play menu item will be displayed to perform installation at the initial start up of the TV when MOD is "on" and after installation is done, VMOD will be automatically set to OFF.

**UKPNP:** UK Plug and Play.

Function: Disable/Enable UK's default Plug and Play setting.

Values: OFF= Disabled, UK's default Plug and Play setting is not available. ON= Enabled, UK's default Plug and Play setting is available.

Note: When UKPNP and VMOD are "on" at the initial set-up, LANGUAGE= ENGLISH, COUNTRY= GREAT BRITAIN and after auto store is complete, VMOD will be set automatically to "off" while UKPNP remain ON.

**Program Selection**

**SURF:** Surf.

Function: Disabled/Enabled surf feature.

Values: OFF= Disabled, Surf feature is not available. ON= Enabled, Surf feature is available.

**SZAP:** Smart Zapper.

Function: Disable/Enable Smart Zapper.

Values: OFF= Disabled. ON= Enabled.

**PLST:** Program List.

Function: Disable/Enable Program List function.

Values: OFF= Disabled, the access to Program List Command is ignored. ON= Enabled, the access to Program List Command is processed.

**Picture In Picture**

**PIPC:** PIP Control.

Function: Disable/Enable submenu to adjust PIP Picture settings

Values: OFF= Disabled, PIP feature is not available. ON= Enabled, PIP feature is available

Note: PIP is present in FEATURES submenu when PIPC is ON. When PIPC is switched OFF, bits PIPT, W4X3, and W169 must be automatically set to OFF.

**PIPT:** PIP Tuner.

Function: To determine the presence of second tuner.

Values: OFF= Disabled, second tuner is not available. ON= Enabled, second tuner is available.

Note: When PIPC is switched OFF, bits PIPT, W4X3, and W169 must be automatically set to OFF.

**W4X3:** DW 4:3

Function: Disabled/Enabled Double window with 4:3 Main Picture.

Values: OFF= Disabled, Double Window with 4:3 Main Picture is not available. ON= Enabled, Double Window with 4:3 Main Picture is available.

**W169:** DW 16:9.

Function: Disabled/Enabled Double Window two compressed 16:9 pictures.

Values: OFF= Disabled, Double Window with compressed 16:9 is not available. ON= Enabled, Double Window with compressed 16:9 is available.

**Clock**

**SMCK:** Smart Clock/Autochron.

Function: Disable/Enable smart clock/AutoChron function.

Values: OFF= Disabled, menu item smart clock function not available. ON= Enabled, menu item smart clock function available.

Note: For NAFTA, AUTOCHRON is present in INSTALL submenu when SMCK is ON. For AP-PAL and EUROPE,

Smart clock downloaded from Teletext is enabled when SMCK is ON.

**NVCK:** Non-Volatile Clock.

Function: Disabled/Enabled Non Volatile Clock function.

Values: OFF= Disabled, non-volatile clock not available. ON= Enabled, non-volatile clock is available.

**TIME:** Timer.

Function: Disable/Enable menu item TIMER.

Values: OFF= Disabled, menu item TIMER not available. ON= Enabled, menu item TIMER available.

Note: TIMER submenu is present in FEATURES submenu when TIME is ON.

**Data Service**

**CCAP:** Closed Caption.

Function: Disabled/Enabled a submenu to set the Caption mode or Text mode, and to enable/disable CC display.

Values: OFF= Disabled menu item CLOSE CAP is not available. ON= Enabled menu item CLOSE CAP. Available.

Note: CLOSED CAP is present in FEATURES submenu when CCAP is ON.

**CTXT:** Caption Text.

Function: Disabled/Enabled Text mode setting.

Values: OFF= Disabled, TEXT mode settings are not available. ON= Enabled, TEXT mode settings are available.

Note: TEXT mode settings (TEXT 1 to TEXT 4) are present in CAPTION MODE menu item in the CLOSE CAP submenu when CTXT is ON.

**DTXT:** Dual Text.

Function: Disable/Enable Dual Text.

Values: OFF= Disabled. Dual text is not available. ON= Enabled. Dual text is available.

**VTXT:** Video Text.

Function: Disabled/Enabled Video Text.

Values: OFF= Disabled, Videotext is not available. ON= Enabled, Videotext is available.

**RCMX:** RC for Teletext Mix Mode.

Function: Disable/Enable RC for Teletext Mix mode support.

Values: OFF= Disabled. RC for mix mode is not available. ON= Enabled, RC for mix mode is available.

**FAPG:** Favorite Page.

Function: Disable/Enable favorite page in Teletext mode.

Values: OFF= Disabled favorite page in Teletext mode. ON= Enabled favorite page in Teletext mode.

**T1H0:** 100-Page Text.

Function: Disable/Enable 100-page Text.

Values: OFF= Disabled. 100-page text is not available. ON= Enabled, 100-page text is available.

**T2H5:** 250-Page Text.

Function: Disable/Enable 250-page Text.

Values: OFF= Disabled. 250-page text is not available. ON= Enabled, 250-page text is available.

**T12H:** 1200-Page Text.

Function: Disable/Enable 1200-page Text.

Values: OFF= Disabled. 1200-page text is not available. ON= Enabled, 1200-page text is available.

**Lock Features**

**CHLK:** Child Lock.

Function: Disable / Enabled function to block/unblock channels.

Values: OFF= Disabled. ON= Enabled.

Note: This option is applicable to EU and AP.

**AULK:** Auto Lock.

Function: Disabled/Enabled Auto Lock.

Values: OFF= Disabled, AUTOLOCK is not available (CHILDLCK is used). ON= Enabled, AUTOLOCK is available i.s.o. CHILDLCK.

**VCBK:** Vchip Block Unrated.

Function: Disabled/Enabled menu item BLOCK UNRATED.

Values: OFF= Disabled, menu item BLOCK UNRATED not available. ON= Enabled, menu item BLOCK UNRATED available

Note: For NAFTA and LATAM, VCHP must be "on" to enable BLOCK UNRATED.

Note: BLOCK UNRATED is present in AUTOLOCK / BLOCKED OPTION submenu when VCBK is ON.

Note: BLOCK UNRATED is present in AUTOLOCK REVIEW screen when VCBK is ON.

**VBNR:** Vchip Block No Rating.

Function: Disabled/Enabled menu item BLOCK NO RATING.

Values: OFF= Disabled, menu item BLOCK NO RATING not available. ON= Enabled, menu item BLOCK NO RATING available.

Note: For NAFTA and LATAM, VCHP must be "on" to enable NO RATING.

Note: NO RATING is present in AUTOLOCK / BLOCKED OPTION submenu when VBNR is ON.

Note: NO RATING is present in AUTOLOCK REVIEW screen when VBNR is ON.

**OSD/Menu Related**

**SOSD:** Smart OSD.

Function: Disable/Enable full display of SMART SOUND and SMART PICTURE OSD.

Values: OFF= Disabled, full display of SMART SOUND and SMART PICTURE OSD not available. ON= Enabled, full display of SMART SOUND and SMART PICTURE OSD available.

**BNUM:** Bar Numeric Items.

Function: Disabled/Enabled the numerical values to be displayed beside the slider bar.

Values: OFF= Disabled, the numerical values is not display beside the slider bar. ON= Enabled, the numerical values is display beside the slider bar.

**STOR:** Store.

Function: Store Picture and Sound settings.

Values: OFF= Disabled, menu item STORE is not available. ON= Enabled, menu item STORE is available.

Note: STORE is present in PICTURE and SOUND submenu when STOR is ON.

**APCL:** Active Control Logo Display.

Function: Enable/Disable the selection of Display logo in the sequence when Active Control key is pressed.

Values: OFF= Disabled, the sequence for Active Control (with wrap around) is Off -> On -> Display On. ON= Enabled, the sequence for Active Control (with wrap around) is Off -> On -> Display On -> Display Logo.

**Miscellaneous**

**SBNP:** Auto Standby with No Picture.

Function: Disable/Enable automatic switch to standby after 15 minutes when no ident.

Values: OFF= Disabled, no automatic switch to standby. ON= Enabled, set switches to standby after 15 minutes when no ident.

**AUSB:** Auto Standby Auto On.

Function: Disable/Enable automatic switch to standby if no RC or local keyboard response after 4 hours provided that the set is "on" from standby mode by the timer.

Values: OFF= Disabled, no automatic switch to standby. ON= Enabled, set switches to standby after 4 hours.

**EPG:** Electronic Program Guide.

Function: Disable/Enable EPG feature.

Values: OFF= Disabled, EPG feature is not available. ON= Enabled, EPG feature is available.

**P50:** P50 (Easylink).

Function: Disable/Enable P50 feature.

Values: OFF= Disabled, P50 feature not available. ON= Enabled, P50 feature is available.

**HOSP:** Hospitality.

Function: Disabled/Enabled hospitality mode.

Values: OFF= Disabled, hospitality mode is disabled. ON= Enabled, hospitality mode is enabled.

**Region**

**TWKE:** Taiwan/Korea.

Function: Select between Taiwan and Korea.

Values: OFF= Korea. ON= Taiwan

**MIDE:** Middle East.

Function: Select Middle East region.

Values: OFF= Non-Middle East. ON= Middle East

Note: This option is also used to differentiate the AP PAL (2AP1) and AP Middle-east (2AP2) clusters. If MIDE is set to OFF, it is referring to 2AP1 cluster. If MIDE is ON, it is referring to 2AP2 Cluster.

**EWEU:** East/West Europe region.

Function: This option is used to allow the development team to trigger the NVM initialization process during the development phase.

Values: OFF= Pressing the Freeze key in the Aux mode will NOT change the password of the NVM. ON= Pressing the Freeze key in the Aux mode will change the password of the NVM. The NVM will be re-initialized with the default values when the TV is wakeup from standby.

Note: This option is only applicable A02E 2003

## 9. Circuit Descriptions, Abbreviation List, and IC Data Sheets

Index of this chapter:

1. Introduction
2. Block diagrams
3. Power supply
4. HDMI
5. Video
6. Synchronization
7. Audio
8. Control
9. Protections
10. Software upgrading
11. Abbreviation list

- As this is a global chassis, the circuit descriptions are meant for all regions. Where necessary, a split up is made per region.
- Only **new** circuits (circuits that are not published recently) are described.
- For the "known" LSP circuits, see the R8 (NAFTA) or EM5 (EU & AP) chassis manual.
- Figures can deviate slightly from the actual situation, due to different set executions.
- For a good understanding of the following circuit descriptions, please use the diagrams in chapter 6 and 7. Where necessary, you will find a separate drawing for clarification.

### 9.1 Introduction

The A02 is intended as the Mainstream TV platform for the years 2003 and 2004 and successor to the A10. Covering three ranges (Digital Ready, Digital Prepared, and Digital Integrated) with screen sizes of 28 inch WS to 36 inch WS RF (16:9) and 29 inch to 38 inch RF (4:3). The platform supports 50 Hz, 100 Hz, and progressive scan.

It is based on the SALSA system (System Application for Lower Segment Analog television), which is a highly integrated solution for TV. The system comprises two ICs: the ADOC (Analog Digital One Chip) and the MPIF (Multi Platform InterFace). The MPIF IC performs analog processing for IF, source selection, and analog to digital conversion. The ADOC IC incorporates video and audio processing as well as the complete TV control functionality. The ADOC aims at the low and mid range market segment.

As one of the first Philips chassis, it is equipped with a HDMI (High Definition Multimedia Interface) connector, for interfacing (HD) digital audio and video sources.

The split-up between an analog (MPIF) and a digital part (ADOC) has the following advantages:

- High frequent parts (IF) can be included in the concept.
- Less A/D and D/A converters needed for source switching.
- Better performance for AD converters (realized in analog design environment, more accurate, less tolerance).
- Critical items like reference voltages can be realized in the analog environment.
- Integrated SCART buffers.

The new A02 chassis has the following features:

- An LSP (Large Signal Panel) that is based on the existing R8 chassis.
- A new SSB (Small Signal Board) with very high integration.
- Upgradeable main software (via ComPair). The software is a large and re-engineered version of the 'MG' software used by Philips CE for several years.

#### 9.1.1 Large Signal Panel

The chassis has a full sized LSP, which is identical to the one in the R8 chassis.

The main functionalities of the LSP are:

- Supply,
- Deflection,
- Sound amplification.

The LSP (single sided) is built up very conventional, with hardly any surface mounted components on the copper side. It has a large "hot" part, including both deflection coils.

#### 9.1.2 Small Signal Board

The SSB is a high tech module (four layer, 2 sides reflow technology, full SMC) with very high component density. Despite this, it is designed in such a way, that repair on component level is possible. To achieve this, attention was paid to:

- Accessibility of the test points. The SSB has good accessible service positions.
- Clearance around surface mounted ICs (for replacing).
- Detailed diagnostics and fault finding is possible via ComPair.
- Software upgrading is possible via ComPair.

The main functionalities of the SSB are:

- Tuner input,
- I/O interface provisions,
- TXT and Control,
- Video and Audio decoding,
- Feature Box,
- Sync and Geometry control.

Further features of the SSB are:

- The PIP functionality (when present) is integrated on the SSB.
- The 3D Comb filter functionality (for USA) is integrated on the SSB.

On the photographs you can see where the key components are located on the SSB (Note: The actual PWB can differ from these photographs. They are only meant to give a general overview):



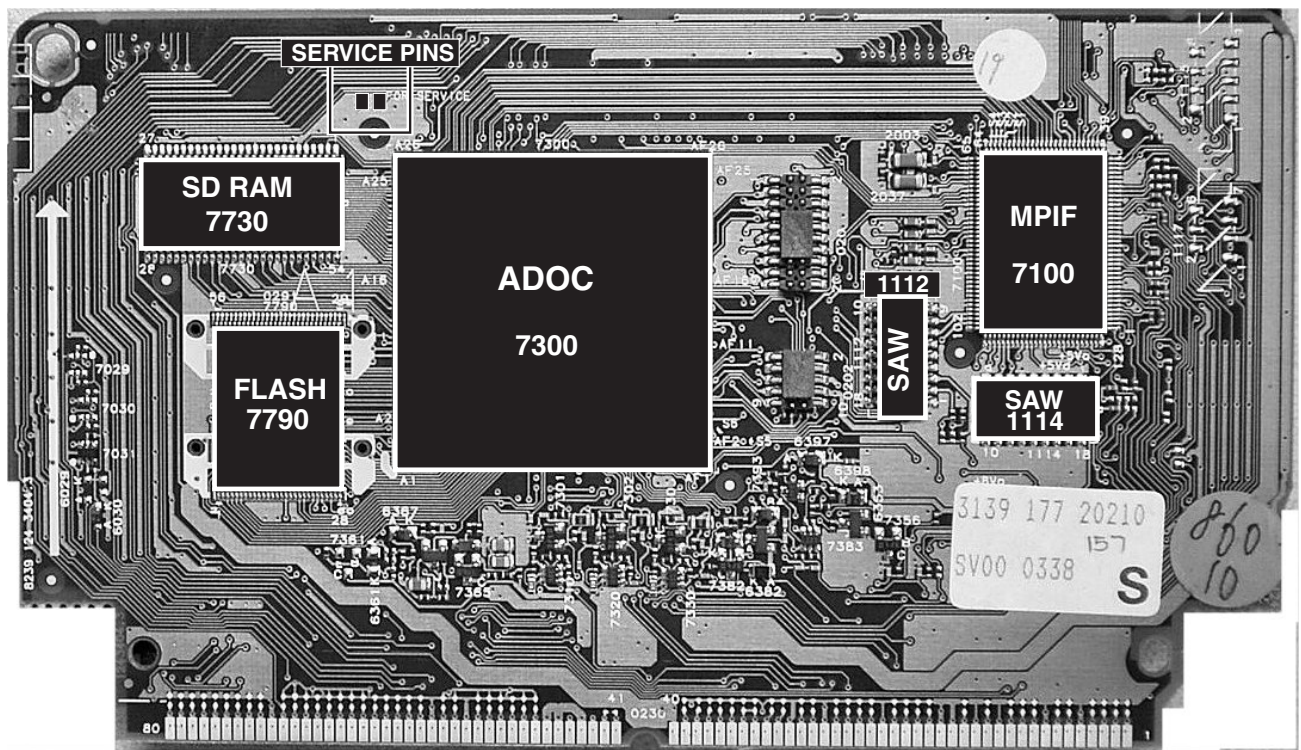
CL 36532058\_060.eps  
281003

Figure 9-1 SSB top view (tuner side)

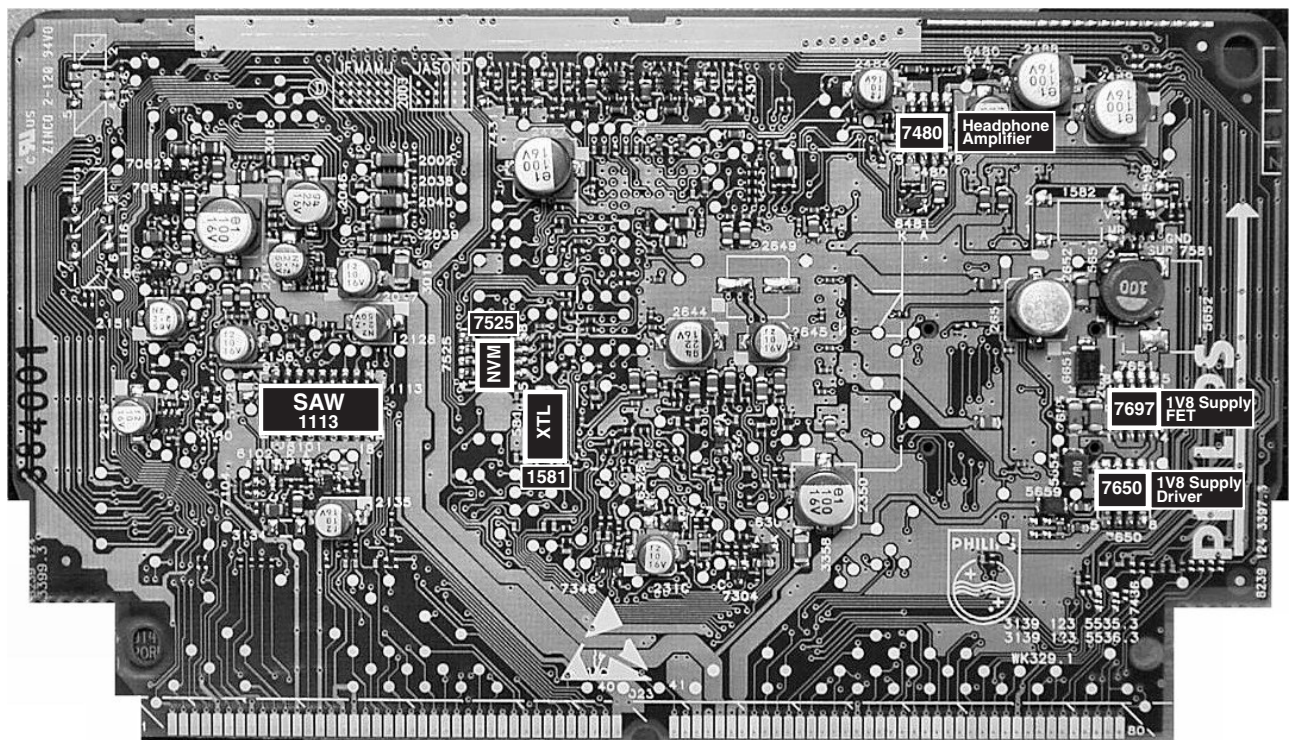
CL 36532058\_061.eps  
271003

Figure 9-2 SSB bottom view (LOT side)

## 9.2 Block Diagrams

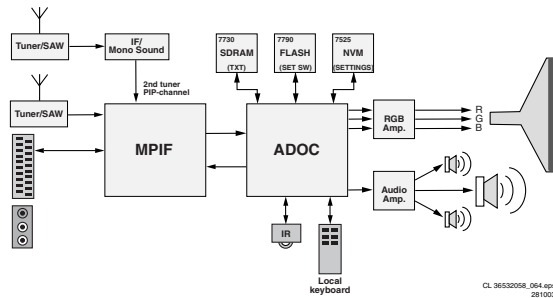


Figure 9-3 Chassis block diagram

The tuner is a PLL tuner and delivers the IF-signal, via a SAW-filter, to the MPIF IC (Multi Platform InterFace). This is an analog video and audio pre-processing unit for the ADOC TV processor. It contains the high frequent IF part and all the analog video and audio source switching for external in- and outputs. The MPIF can handle CVBS, Y/C, RGB (1fH/2fH) and YPbPr (1fH/2fH) video signals as well as stereo, I2S, and second sound IF audio signals. The MPIF converts the selected video and audio streams from the analog to the digital domain. Via three high-speed serial data links (I2D), the digitized audio and video signals are streamed to the ADOC IC for further processing.

The ADOC (Analog Digital One Chip) is a fully integrated, digitally implemented TV processor for audio, video, VBI (Vertical Blanking Interval) services, graphics, and control. It is a global, multi-standard system primarily designed for the reception and processing of analog broadcast signals. Internal video processing is done in the ADOC with YUV-signals. It also handles the video control, geometry part, and the insertion of the TXT/CC/OSD RGB-signals. The video part delivers the RGB signals to the CRT-panel and the geometry part delivers the H-drive, V-drive (differential output), and E/W-drive.

An integrated MIPS 1910 processor runs the chassis software and takes care of the set control, error generation TXT/CC/OSD input-, and output processing. The NVM (Non Volatile Memory) is used to store the settings, the Flash-RAM contains the set software, and the SDRAM stores the Teletext pages (in some versions, this is stored in the internal memory of the ADOC).

Both deflection circuits are located on the LSP and are driven by the ADOC. The horizontal output stage generates also some supply voltages and the EHT-, focus- and Vg2-voltages.

The RGB amplifiers on the CRT-panel are integrated in one IC and are supplied with 200 V from the LOT. The SCAVEM circuit modulates transitions of the Luminance (Y) signal on the horizontal deflection current, giving a sharper picture.

Sound IF processing, audio source selection, and audio analog-digital signal conversions are done in the MPIF IC. The ADOC contains a digital TV sound processor for analog and digital multi-channel sound systems in TV sets. By hardware programming, several applications can be scaled. The audio output stage is built around a balanced amplifier, and is located on the LSP. It uses a monolithic integrated power amplifier IC, the TDA7497. The gain of the amplifier is constant. This means that volume control is done via the ADOC.

There is a separate Standby Supply, in order to reduce the Standby power consumption. During Standby, the Main Supply is switched "off" (via TS7529).

A relay (1550) is used to switch the Degaussing circuit. It is switched "on" after set start-up and switched "off" by the microprocessor after 12 s.

The Main Supply, a SMPS based on the "boost converter" principle, generates the 140 V (V\_BAT) and the +/- 28 V for the audio part.

## 9.3 Power Supply

### 9.3.1 Introduction

The power supply circuitry is located on the large signal PWB, together with the audio amplifier and the deflection. It comprises of:

- Mains entrance with fuse.
- Separate standby -supply.
- Mains harmonic circuit.
- Mains rectifier.
- Main-supply: is able to deliver a continuous power between 100 W and 160 W.
- Degaussing.

For a detailed circuit description, see the R8 (NAFTA) or EM5 (EU & AP) Service Manual.

### 9.3.2 Power Supply architecture

The A02 SSB is supplied by +5V, +5.2V, +3.3V and +8V supply lines from the LSP. The SSB contains:

- A DC/DC converter which steps down +5.2V to +1V8,
- A switch to cut off the 3V3 supply to the 3D Comb in "Standby" mode, and
- A regulator to generate the 2V5.

When the set is in "Power STANDBY" mode, the +5.2V, +3.3V supply lines are present. Consequently, only the ADOC IC (+3V3 and +1V8), the SDRAM (+3V3), the Flash memory (+3V3), and the NVM memory (+3V3) are supplied. Other than NVM, all the other devices are powered down in "Standby" mode. See section below for more details on the power modes.

#### OFF Mode

The set is completely switched "off" from the mains. This is done with the mains switch for Europe and AP (for NAFTA it would mean disconnecting the TV from the mains by pulling out the mains cable). Depending upon the last Standby Status (stored in NVM), this mode can transit to "on" mode or "STANDBY" mode.

The transition timing for a Cold start from "off" state to "on" shall be such that from the instance the ADOC gets a hard reset, within 3 seconds one will hear the audio and within 7 seconds one will see the picture.

#### ON Mode

This is the normal operating mode. All the power supply lines on the A02 SSB and LSP are available. All the circuits in the set are active. From this mode, it is possible to transit to "STANDBY", "SEMI-STANDBY", "PROTECTION", or "OFF" mode.

#### STANDBY Mode

The total power consumption of the TV set in this mode is equal or less than 1 W. The LED will indicate the Standby state. In this state only the ADOC, SDRAM, Program Memory, NVM, and all means to wake-up the set are powered. Rest of the A02 sub-systems is disconnected. A STANDBY control port controls this.

The transition timing from "STANDBY" to "ON" state is such that within 3 seconds, one will hear the audio and within 7 seconds, one will see the picture. From this mode, it is possible to transit to "ON", "SEMI-STANDBY", or "OFF" mode.

#### SEMI-STANDBY Mode

All the circuits in the set (ADOC, MPIF, etc), except the Audio output, Deflection, and hence CRT display, are powered up and fully active. The Audio Mute is activated. The set, however,



will appear to behave and to look like "STANDBY" mode to the user. The user is totally oblivious of the existence of this mode. The status of the power supply lines and the estimated total power consumption of the SSB are the same as "ON" mode. In this mode, the ADOC ICs horizontal deflection drive output is disabled, while the STANDBY control port is disabled. This consequently causes the LOT stage on the LSP to be inactive (although  $V_{batt}$  voltage is present) that, in turn, will cause the EHT to be cut off. This in turn will cause the CRT display to be inactive.

From this mode, it is possible to transit to "ON" mode, "STANDBY" mode, "PROTECTION" mode or "OFF" mode.

**PROTECTION Mode**

Power profile for protection mode is as low as required to allow "soft" diagnostics, error detection, and to indicate LED flashes to flag the type of fault. The horizontal deflection is "off" in this mode. From the protection mode, the only possible transition is to "OFF" mode.

### 9.3.3 Start Up Sequence

1. When we start the set (cold start), initially 5V2, 3V3, and 1V8 will be available. These come from the Standby module of the power supply.
2. After this, the microprocessor resets (tied to 1V8 and 3V3 supplies) and checks the last status of the supply from the NVM. Accordingly, the set will be put in "STANDBY" or in the normal "on" condition.
3. Now, 5V and 8V are available if the last status was "on" condition, and the DOP is initialized by the microcontroller through the PI bus (not via the I2C).
4. The H-drive will become available from the DOP, which is the source for the "SUP\_ENABLE" signal.
5. Via the "SUP-ENABLE" signal, the Main Supply is switched "on" and will deliver the V\_BAT to the Line deflection stage.
6. EHT generation is now started.
7. The uP will un-blank the picture.
8. When you switch "off" the set, this is done in a controlled way via the POR (Power On Reset) signal.

**Note:** Standby is controlled by the STANDBY Line of the uP (not by the DOP).

### 9.3.4 Shut Down Sequence

This section describes the processes that need to be handled by hardware and software when power is disconnected from the set.

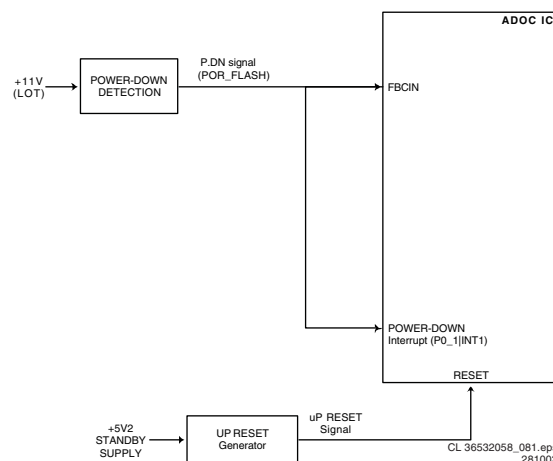
Some system requirements:

- To handle CRT discharge.
- To handle "switch off" plops.
- To prevent NVM corruption at switch "off".
- To effectively distinguish between the condition of mains interruptions and shutdown and handle them properly.
- The "power down" detection is acquired from the deflection supply (+11V) and the level is translated to +3.3V (this event has the highest interrupt priority to trigger SW shutdown procedure).
- Power down detection is fed to the FBCIN input, initiates a slow stop, and hence ensures CRT discharge (it is important that the slow-stop is maintained for at least 50 ms to assist good discharge).
- The microcontroller, hence the system, shall have a clean power "on" and power "off" reset with respect to its supply. The microcontroller shall not be operational when the supply voltage is below the recommended limits. The transition between active and reset is fast.
- The microcontroller "off" reset must occur much later (> 45 ms) than the POWER DOWN signal (P.DN).

When the POWER DOWN interrupt occurs, there is no way of knowing whether it is due to Medium Mains Interruptions or due to shutdown. Hence, there is no choice but to initiate shutdown

procedure as described further below. The definition of Mains Interruption is given below:

- **Short Mains Interruptions.** Duration of the interrupts  $\leq$  55 ms. The set shall continue to work properly. The "power off" acquisition circuit shall filter such events.
- **Medium Mains Interruptions.** Interruptions are of the order 70 to 80 ms. This is a typical situation when the "power off" acquisition circuit, signals that the power is going down but the microcontroller does not get a reset. In this condition, a POWER DOWN signal is generated but no POWER OFF RESET signal is available.
- **Long Mains Interruption or Shutdown.** Any interrupt above 80 ms shall cause a microcontroller reset and hence a cold start. This happens, when the power is disconnected long enough to get a "Power Off Reset" as well as the microcontroller reset. After this situation, the system would automatically cold start when the power resumes.



**Figure 9-4 Shut down block diagram**

### **Shutdown Procedure**

1. Exclude all processes and do not respond to any interrupts - including RC events. However, during the following defined conditions of stopping the deflection (DFL-bit= 0), ignore the P.DN interrupt and rest of the procedure:
  - The system switched from ON to Standby by the user.
  - Protection event that forces the H-Deflection to stop.
  - Any other SW controlled event that causes the deflection to stop.
2. Since the P.DN signal is connected to FBCIN input, the DOP should stop slow immediately - no software intervention is required. The precondition for this is that the FBDM bit in DOP is set to "1". The slow -stop process will continue for the next 40 ms or so.
3. Mute Audio Output / Sound Enable line.
4. Mute audio external outputs (in ADOC).
5. Set the DFL-bit to "0", such that deflection shall not restart after the slow -stop process is done.
6. Disable NVM access. Do the following:
  - Put the NVM in standby state to stop I2C write to NVM, by sending the Universal Reset Sequence.
  - Set Write Enable high: this avoids any further Write sequence to the NVM.
7. Disable all the I2C hardware communication.
8. Wait for 200 ms and execute a cold start when there is no microcontroller-reset signal. This is considered as "medium mains interruption".
9. After the cold start, the set should resume to the last status of user settings.

## 9.4 HDMI

### 9.4.1 Introduction

**Note:** Text below is an summary from the "HDMI Specification" that is issued by the HDMI founders (see <http://www.hdmi.org>).

The High-Definition Multimedia Interface is developed for transmitting digital television audiovisual signals from DVD players, set-top boxes and other audiovisual sources to television sets, projectors and other video displays. HDMI can carry high quality multi-channel audio data and can carry all standard and high-definition consumer electronics video formats. Content protection technology is available. HDMI can also carry control and status information in both directions.

As shown in the HDMI block diagram, the HDMI connector carries four differential pairs that make up the TMDS (Transition Minimized Differential Signaling) data and clock channels. These channels are used to carry video, audio, and auxiliary data. In addition, HDMI carries a VESA DDC channel. The DDC is used for configuration and status exchange between a single Source device and a single Sink device.

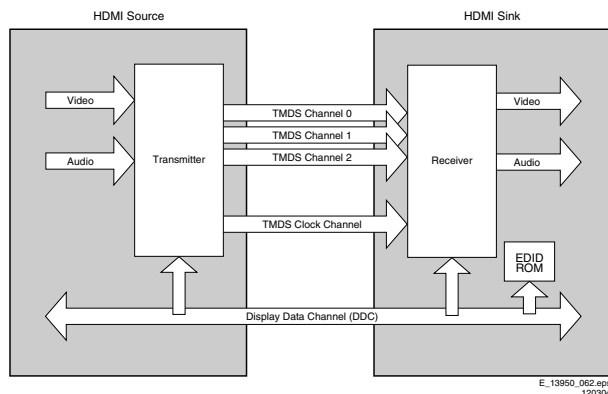


Figure 9-5 HDMI block diagram

Audio, video, and auxiliary data is transmitted across the three TMDS data channels. The video pixel clock is transmitted on the TMDS clock channel and is used by the receiver as a frequency reference for data recovery on the three TMDS data channels.

Video data is carried as a series of 24-bit pixels on the three TMDS data channels. TMDS encoding, converts the 8 bits per channel into the 10 bit DC-balanced transition minimized sequence, which is then transmitted serially across the pair at a rate of 10 bits per pixel clock period.

Video pixel rates can range from 25 MHz to 165 MHz. Video formats with rates below 25 MHz (e.g. 13.5 MHz for 480i/NTSC) can be transmitted using a pixel-repetition scheme. The video pixels can be encoded in either RGB, YCBCR 4:4:4, or YCBCR 4:2:2 formats. In all three cases, up to 24 bits per pixel can be transferred.

In order to transmit audio and auxiliary data across the TMDS channels, HDMI uses a packet structure. In order to attain the higher reliability required of audio and control data, this data is protected with a BCH error correction code and is encoded using a special error reduction coding to produce the 10-bit word that is transmitted.

Basic audio functionality consists of a single IEC 60958 audio stream at sample rates of 32 kHz, 44.1 kHz or 48 kHz. This can accommodate any normal stereo stream. Optionally, HDMI can carry a single such stream at sample rates up to 192 kHz or from two to four such streams (3 to 8 audio channels) at sample rates up to 96 kHz. HDMI can also carry IEC 61937

compressed (e.g. surround-sound) stream at sample rates up to 192 kHz.

The DDC is used by the Source to read the Sink's Enhanced Extended Display Identification Data (E-EDID) in order to discover the Sink's configuration and/or capabilities.

### 9.4.2 Implementation

HDMI input signals are fed to the HDMI Panellink Receiver (item 7002 on diagram M1). This IC consists of a flexible audio and video interface.

The video part delivers RGB/YPbPr output, that directly is fed to the MPIF source selector on the SSB (The IC is also capable of RGB input, assuring backwards compatibility with DVI).

The audio part delivers a 2-channel I2S digital audio signal that is fed to the audio DAC (item 7011). After DA conversion the signals are also fed to the MPIF source selector.

## 9.5 Video

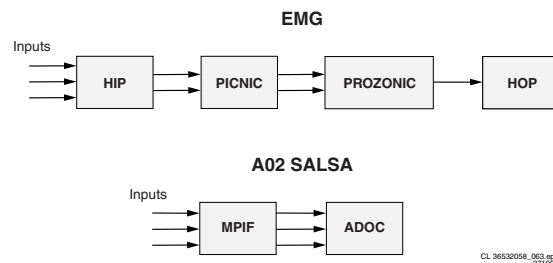


Figure 9-6 Signal processing A02- versus EMG-chassis.

The SALSA video processing part is a highly integrated solution. It comprises only two ICs, the ADOC (Analog Digital One Chip) and the MPIIF (Multi Platform InterFace), while in the R8-chassis, this was handled by four ICs (HIP, PICNIC, PROZONIC, and HOP).

The MPIIF uses a nominal 8 V and 5 V supply, while the ADOC requires nominal supplies of 1.8 V and 3.3 V.

The video processing of the SALSA system can be split into six parts:

- Initial source selection and analog to digital conversion performed by MPIIF.
- Demodulator (VIDDEC) performed by the ADOC.
- Front End Features (FEF) performed by the ADOC.
- Memory Based Features (MBF) performed by the ADOC.
- Back End Features (BEF) performed by the ADOC.
- Digital Output Processing (DOP) performed by the ADOC.

### 9.5.1 MPIIF Analog Frond End

#### Introduction

The MPIIF (Multi Platform InterFace, type number PNX3000, item number 7100) is an analog video and audio pre-processing unit for the ADOC TV processor. It contains the high frequent IF part and all the analog video and audio source switching for external in- and outputs. The MPIIF can handle CVBS, Y/C, RGB (1fH/2fH) and YPbPr (1fH/2fH) video signals as well as stereo, I2S, and second sound IF audio signals. The MPIIF converts the selected video and audio streams from the analog to the digital domain. Via three high-speed serial data links (I2D), the digitized audio and video signals are streamed to the ADOC IC for further processing. Following figure shows the MPIIF block diagram.

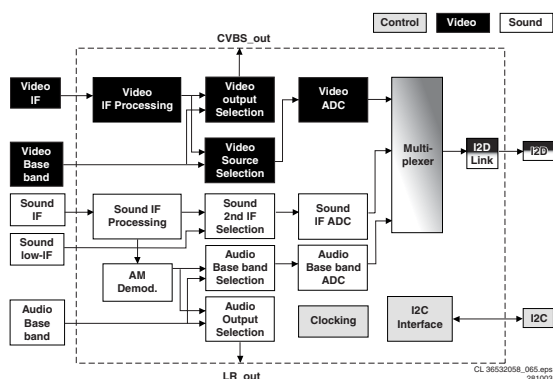


Figure 9-7 MPIF block diagram

Some MPIF features:

- IF Processing:
  - Amplifier, AGC.
  - Down mixer to base band.
  - Sound trap, low pass filter.
- Video base band switching:
  - CVBS, Y/C.
  - RGB, YPbPr (1fH/2fH).
- Audio base band switching.
- Video and audio A/D conversion.
- I2D formatter:
  - Data transfer to ADOC.

#### Vision IF

The video signal is demodulated by means of an alignment-free PLL carrier regenerator with an internal VCO. This VCO is calibrated by means of a digital control circuit, which uses an external crystal frequency as reference. The frequency setting for the various standards (33.4, 33.9, 38.0, 38.9, 45.75 and 58.75 MHz) is realized via the I2C bus.

The AFC output is generated by the digital control circuit of the IF-PLL demodulator and can be read via the I2C bus.

The AGC-detector operates on top sync or top white level.

The MPIF IC has an integrated sound trap filter. The trap frequencies can be switched via the I2C-bus.

Also, a group delay correction filter is integrated. The filter can be switched between the PAL BG curve and a flat group delay response characteristic. This has the advantage that in multi-standard receivers the video SAW filter does not need to be switchable (cost effective).

#### Sound IF

The MPIF has a separate sound IF input to enable Quasi Split Sound (QSS) applications. The sound IF amplifier is similar to the vision IF amplifier and has a gain control range of about 55 dB.

The AGC detector measures the SIF carrier levels (average level of AM or FM carriers) and ensures a constant signal amplitude for the AM demodulator and QSS mixer.

For applications without SIF SAW filter, the IC can also be used in intercarrier mode. In this mode, the composite video signal from the VIF amplifier is fed to the QSS mixer and converted to the intercarrier frequency. AM sound demodulation is realized in the analog domain with the QSS mixer.

#### Source Selection

The following selector parts can be identified:

- **CVBS/YC source selector.** The video input selector consists of four independent source selectors, that can select between the CVBS signal coming from the IF part and four external CVBS signals. Two of the external CVBS inputs can also be used as YC input. One selector is used for selection of the primary video channel. A second selector selects the CVBS or YC signal for the secondary channel. The third and fourth selectors are used for

selection of analog CVBS outputs A and B for SCART or line output. The primary channel can be a CVBS or YC signal. If an YC signal is selected for the secondary channel or external CVBS outputs A or B, the luminance and chrominance signals are added so that a CVBS signal is obtained. The video identification circuit detects the presence of a video signal on the CVBS\_IF input (CVBS0). The identification output can be read via I2C bus and is normally used to detect transmitters during search tuning.

- **RGB/YPbPr source selector.** The IC has two RGB inputs. Both inputs can also be used as YPbPr input for connection of video sources with an YPbPr output like a DVD player. The RGB inputs can also be used for fast insertion of RGB signals (for instance on screen display menu's) in the primary CVBS signal. The fast insertion switch is located in the digital video processor. The RGB signals are converted to YUV before further processing. The YUV output signal is digitized with the help of two A to D converters. The U and V components have half the bandwidth of the Y signal, because the U and V signals are multiplexed and digitized with the help of one A to D converter.

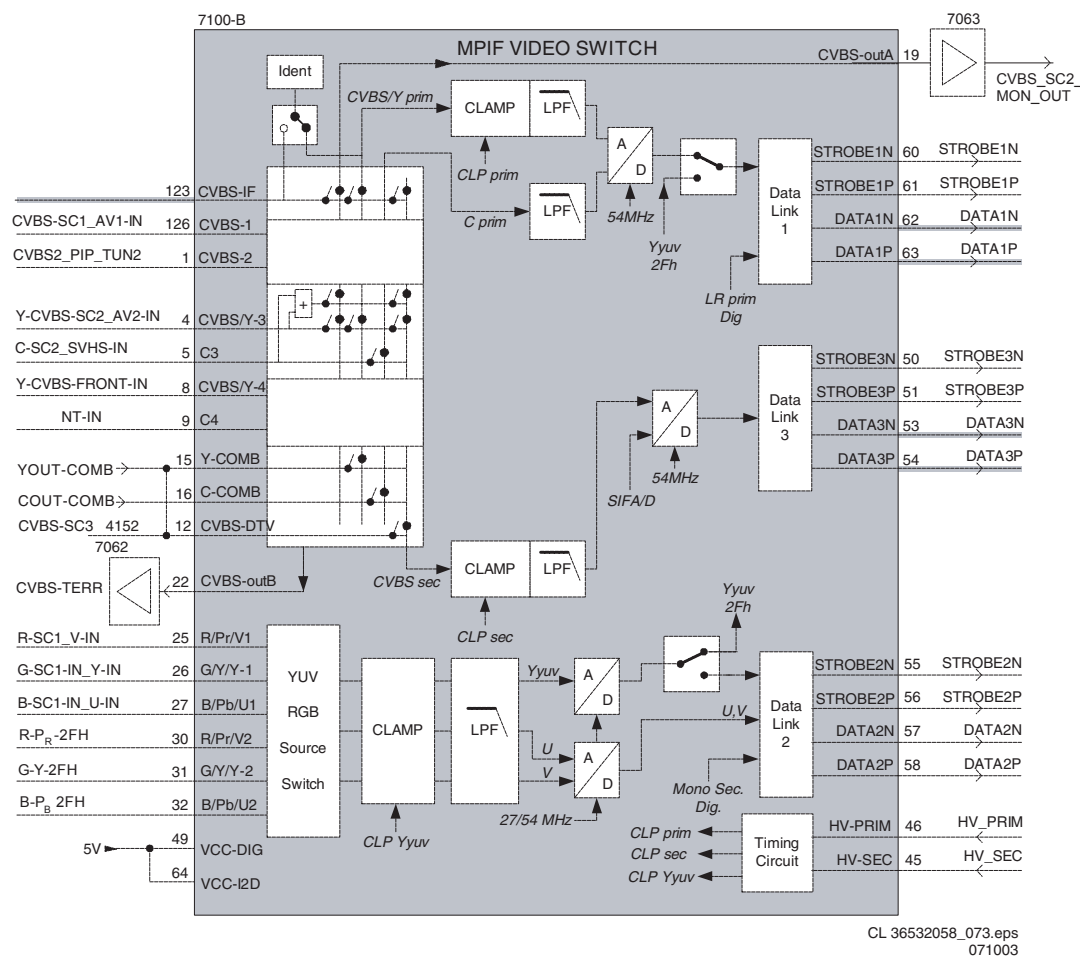


Figure 9-8 MPIF Video source selection

- **Audio source selectors.** The MPIF contains two different audio source selectors. The first selector selects which audio signals are routed to the audio ADCs for further processing in the digital domain. The selector has two outputs, a primary channel and a secondary channel:
  - The primary audio channel is used for one stereo signal. The secondary audio channel can carry a second stereo signal or AM sound signal.
  - The second selector selects which audio signals are fed to the analog audio outputs for SCART (EU only) and line out. This selector has also two stereo inputs for demodulated sound signals coming from the digital video processor.

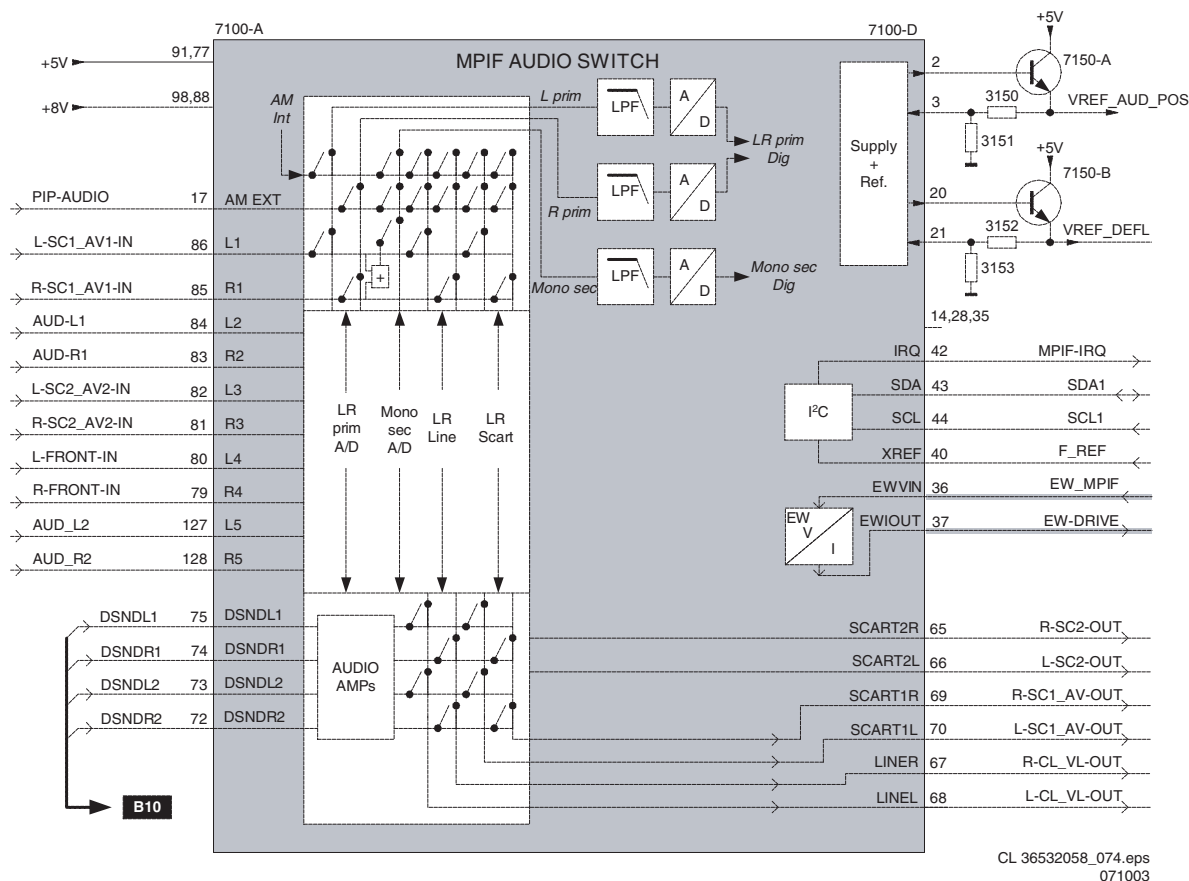


Figure 9-9 MPIF Audio source selection

### A to D Converters

The MPIF contains four video ADCs for analog and digital video broadcast signals. The clock frequency for these ADCs is either 27 MHz or 54 MHz. In some cases, two analog signals are multiplexed at the input of one ADC. In these cases, the clock frequency of the ADCs is 54 MHz, while the sample frequency for each of the two signals is 27 MHz.

The sample frequency for standard 1fH video signals is 27 MHz.

For the YUV channel the sample frequency of the U and V components is half the sample frequency of the Y signal. For 2fH YPbPr or RGB input signals (for instance 480p or 1080i ATSC signals), the frequency that is used to sample the YUV signals is twice as high as for 1fH signals. The sample frequency is 54 MHz for Y and 27 MHz for U and V.

Due to the high sample frequency, two data links are needed for transport of the video data to the digital video processor.

### 9.5.2 Data Link Interface (I2D)

The digital interface between MPIF and ADOC is called Data Link (or I2D Link). Data Link is a pin efficient, EMC friendly and power efficient serial interface that transfers the data from MPIF to ADOC over three Data Link interfaces. Each Data Link has a data signal and a strobe signal. The synchronization information is distributed over the data and the strobe signal. To minimize EMC, both signal outputs are low voltage differential swing signals, with a swing of about 300 mV. Each Data Link has four lines, one differential pair for the data, and one differential pair for the strobe. The data rate is 594 Mbit/s. Each Data Link can carry two 27 MHz sampled video

streams (or one 54 MHz sampled 2fH video stream) and two audio channels sampled at 6.75 MHz.

In the MPIF, the (video and audio) data to be transmitted is multiplexed in an output register of 42 bits. The content of that 42 bits register is serial transmitted on one of the three data links. In the ADOC, the serial data is de-multiplexed into parallel streams. The data on the data link is divided in several groups of signals (video, audio and strobe signals). Obvious it is important that the transmitter and receiver are in the same transmitting mode.

### 9.5.3 ADOC Digital TV Processor

#### Introduction

The A02 system is built around the ADOC IC. This chip implements all TV functions in digital technology. Only a few functions (like AD-conversion, IF processing and source select) are implemented in an analog companion IC, the MPIF. The ADOC (Analog Digital One Chip, type number PNX3001-3008, item number 7300) is a fully integrated, digitally implemented TV processor for audio, video, VBI services, graphics, and control. It is a global, multi-standard system primarily designed for the reception and processing of analog broadcast signals.

An integrated MIPS 1910 processor runs the chassis software. This software is stored in a non-volatile external flash memory (item 7790). Following figure shows the ADOC block diagram.



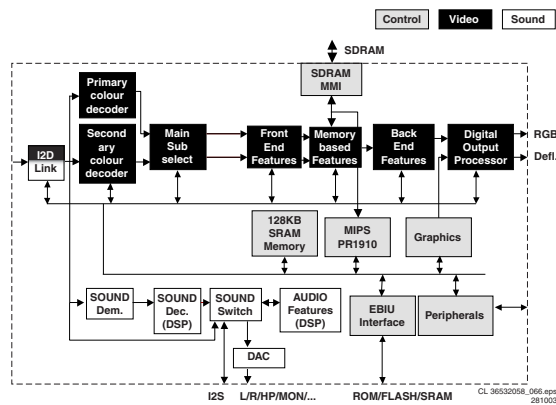


Figure 9-10 ADOC block diagram

The dual stream architecture of the ADOC system allows audio and video processing of two A/V sources simultaneously. The two video streams can be displayed in several programmable ways (main screen, PIP or DW). The two audio streams are audible via the TV loudspeakers and/or the headphones. For the memory-based features (like scan rate conversion, 3D-Comb filtering, dynamic noise reduction, and PIP/DW applications), external SDRAM is used (item 7730). The ADOC also has 128 kBytes of internal SRAM memory. This memory is used to run low latency, timing critical parts of the software. The internal memory is also used if the system operates in a single scan 50/60 Hz interlace application without any other kind of memory based features. Under these circumstances, no external SDRAM is needed.

Some ADOC features:

- Video Decoding:
  - 2-Colour Decoder (PAL, NTSC, SECAM).
  - 2D and 3D Comb filter.
- Memory Based Features:
  - PIP/DW, DNR, Scan Rate conversion.
- Picture Improvements:
  - CTI, LTI, Color correction.
- Digital Output Processor:
  - RGB processing, Scavem, Deflection control.
- Audio Processing:
  - Demodulator/Decoder (A2, NICAM, BTSC).
  - Tone, Volume, Balance, Dolby ProLogic.
- VBI (Vertical Blank Interval) Services:
  - Teletext or Closed Caption, V-chip.
- TV Control:
  - I2C, UART, IR, Keyboard.
- Graphics:
  - Character based.

#### Video Decoding (VIDDEC)

The Video Decoder (VIDDEC) is the video input processor and color decoder. There are two VIDDECs: the primary and the secondary VIDDEC. The VIDDEC processes all CVBS, Y/C, and 1fH/2fH component (e.g. RGB) video input signals.

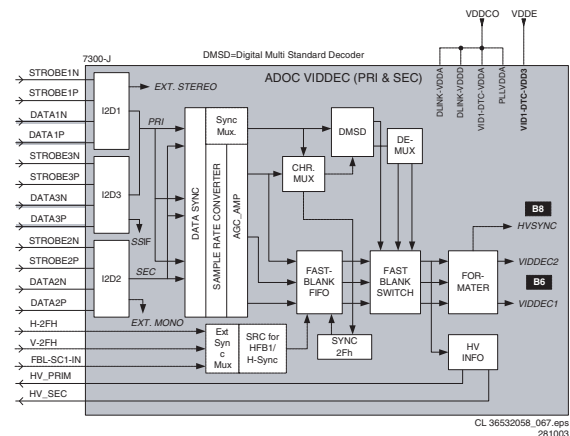


Figure 9-11 VIDDEC block diagram

#### Primary VIDDEC (1fH/2fH)

The primary VIDDEC supports the following functionality:

- Conversion of the digitized samples from MPFI into orthogonal samples (meaning fixed number of pixels per line, independently of line frequency).
- Correction for any amplitude errors of the input signals (CVBS, YC, or YCbCr) by means of an Automatic Gain Control (AGC).
- Standard detection of PAL/NTSC or SECAM and various 1fH/2fH component input formats.
- Color decoding for PAL, NTSC, or SECAM input signals.
- Sync identification (to be used for channel search).
- Sync processing for any 1fH or 2fH input signal.
- Fast-blank insertion of RGB signals (supplied via MPFI) on CVBS input signals.
- 2D Comb filtering. 3D Comb filtering is implemented in the Memory Based Feature block of the Feature Box.

#### Secondary VIDDEC (1fH)

The secondary VIDDEC is mainly intended for use with PIP/DW. It supports the following functionality:

- Conversion of the digitized samples from MPFI into orthogonal samples (meaning fixed number of pixels per line, independently of line frequency).
- Correction for any amplitude errors of the input signals (CVBS) by means of an Automatic Gain Control (AGC).
- Standard detection of PAL/NTSC or SECAM and various 1fH component input formats.
- Color decoding for PAL, NTSC, or SECAM input signals.
- Sync identification (to be used for channel search).
- Sync processing for any 1fH input signal.
- CVBS 1fH input signals only.

#### Data Synchronizer and Sample Rate Converter

The data synchronizer is a de-multiplexer that separates the UV stream into a separate U and V data stream. The sample rate converter converts the video samples from the crystal clock domain to the so-called line locked clock domain, 720 pixels per line.

#### Automatic Gain Control (AGC)

The AGC amplifier block controls the gain of the signal and is controlled directly by the chassis software. This gain will depend on the amplitude of the output signal (signal amplitude and/or sync amplitude) as measured by the AGC gain block. As a secondary function, it controls both the offset at the input and the offset at the output of the gain control.

*Digital Multi Standard Decoder (DMSD)*

This DMSD block contains the following functionality:

- Decodes a CVBS or Y/C (primary VIDDEC) signal and converts it to an YCbCr signal format. All world color standards are supported.
- YC detection (primary VIDDEC) via a SW algorithm.
- 50/60 Hz, interlace/progressive, field polarity, and no-YC detection.
- A chroma notch with programmable width.
- 2D Comb filter (primary VIDDEC). The 3D Comb filter uses the attached SDRAM memory and is implemented in the FBX.
- Macro vision detection.

*Comb Filter*

The ADOC 2D comb works purely in the vertical direction, but can bypass the entire signal as luminance straight away. The 2D comb uses the 180 degrees phase shift of the color carrier between successive lines or two lines apart. Adaptive two or four delay lines 2D Y/C comb filtering is only possible for sources routed onto the Main-Video path.

In the 3D comb filter implementation (for USA only), the 2D comb filter processing in ADOC IC (on the Main-Video path) is disabled via SW. The signal input for the 3D YC comb-filter circuit is derived from the CVBS-SC2\_MON-OUT signal path. The processed signal is re-inserted back via YCOMB and CCOMB inputs of the MPIF IC.

The 3D Comb filter is integrated in one IC (type uPD64083). The block diagram of the 3D Comb panel is indicated in the next figure (re-use of R8 manual, does not reflect the actual circuit **exactly**).

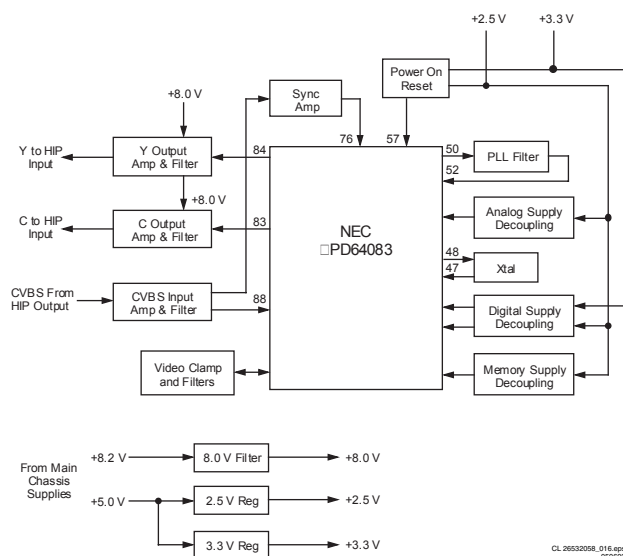


Figure 9-12 Block diagram 3D comb filter

*Standard Detection*

The Standard Detection part identifies PAL/NTSC/SECAM/BW but also involves Horizontal and Vertical sync identification (both 1fH and 2fH) as well as YC detection (via a SW algorithm).

*YUV Multiplexer*

The YUV mixer selects between the YUV output of the DMSD and 1fH component video input signals (RGB, YPbPr) or 2fH input signals (RGB, YPbPr, ATSC). The YUV mixer can also be controlled via a fast blanking input (SCART) to insert RGB signals, such as descrambler OSD or full RGB insertion of DVD players.

When a 2fH input signal is selected as an input, the complete primary VIDDEC is running at 2fH (54 MHz), including DMSD

(in this scenario, the DMSD cannot be used any more for CVBS input signals, and as such, VBI data slicing cannot be done).

*Feature Box*

The Feature Box (FBX) in the ADOC can be divided into three functional parts: The front-end features (FEF), memory-based features (MBF), and back end features (BEF).

The FEF part of the FBX implements all signal analysis functions as well as black stretch and histogram correction. The MBF part applies spatial scaling, temporal noise reduction and up-conversion to either progressive scan or a double field rate (100 Hz).

The BEF part implements spatial picture enhancement functions like sharpness and color enhancement functions, sharpness measurement and horizontal scaling and panorama. The FBX has two video inputs coming from VIDDEC 1 and 2, and outputs one RGB video stream to the display output processor (DOP).

The following sections describe the three functional parts of FBX in more detail.

*Front End Features (FEF)*

The FEF consists of several signal analysis functions (HME, BLD, BBD, NEST), histogram correction (HMO) and black-stretch (BS). Following figure shows the functional block diagram of the video front-end features (FEF). All signal processing in the FEF is nine bits based.

The FEF has two video inputs coming from the VIDDECs. For every block, one video source can be chosen as input, independently for every block. The FEF has two video outputs, designated as "main" and "sub".

Histogram modification can only be performed on the main channel; therefore, the HME block is general connected to the same video source as the main channel. Besides the two VIDDEC inputs, there is also a third virtual input, the "blanking" input. Only main and sub can be connected to this blanking input, and at the same time, it can be specified which sync source has to be used (VIDDEC1 or VIDDEC2).

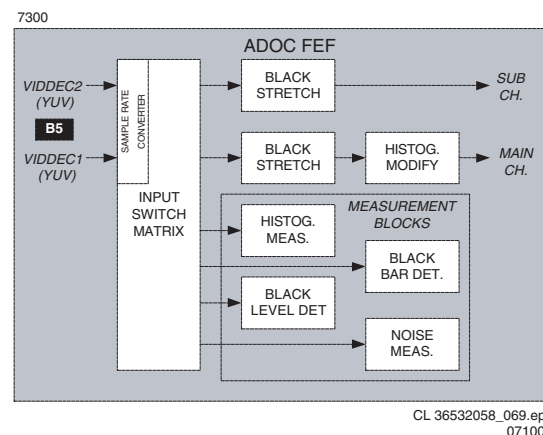


Figure 9-13 FEF block diagram

When a single stream is displayed, the main output is used for this stream. Also, all signal analysis functions should be connected to the same VIDDEC as the main channel is connected to.

When two streams are displayed, then there are two user scenarios: Picture In Picture (PIP) and Double Window (DW). In the PIP scenario, the full screen picture is displayed via the main channel, and the PIP stream is switched to sub. In the DW scenario, selection of the video sources for main and sub depends on if the two streams have a different vertical resolution and how the system has to cope with this difference.

Following blocks are present:

- **Black Stretch (BS).** The function of BS is to pull the dark areas in a picture to even darker levels. BS is available in both the main and sub channel.
- **Histogram (HMx).** This block measures of every field in a programmable (measurement-) window the histogram of the luminance signal. The measurement window is set-up such that the area that contains the subtitles or black bars does not contribute to the histogram.
- **Black Bar Detection (BBD).** Many broadcasts or software played on TVs produce a so-called "letterboxed" picture. Black bars appear above and below the picture. Due to bad standardization of the aspect ratio, e.g. the size of the black bars, there is a need to actively analyze the picture and determine if the picture is in letterbox format and what the size of the black bars is. Black bars are detected by determining if a defined number of pixels (analyzed within a programmable window located in active video) are black. The output of the BBD is the first non-black line and the last non-black line.
- **Black Level Detection (BLD).** The BLD determines within a programmable (measurement) window the "black level" of a picture. The BLD will be used for the BS, but if required, it can also be used for the BBD. The BLD function records in multiple small windows within the measurement window the maximum luminance. The minimum luminance level of the various recorded maximum luminance levels is the true black level. By measuring the maximum luminance level in a small window, the BLD is not sensitive to "black" spikes.
- **Noise Estimation (NEST).** The NEST block analyses the video and outputs a number correlating to the amount of noise in the picture. A basic problem is that picture detail is also 'recognized' as noise. Several control- and status-registers are added to compensate this. The video signal is only analyzed when it is within a programmable (measurement) window. This window coincides with a rectangular shaped part of the (visible) picture. Normally this is the centre part of the picture.

#### Memory Based Features (MBF)

The Memory Based Features (MBF) block embodies a set of functions that require (shared) memory.

The main and sub video streams can be spatially compressed in order to produce a mixed output in the form of several PIP combinations or DW.

The main video stream can be passed through a temporal noise reduction circuit (DNR).

The 3D Comb filter is also implemented in this block.

The main and sub streams are merged when reading from memory. The merged video stream can be up-converted to either a double line rate (progressive scan) or to a double field rate (100 Hz). The up-conversion is done by means of a digital scan function. Following figure shows the functional block diagram of the video memory based features (MBF).

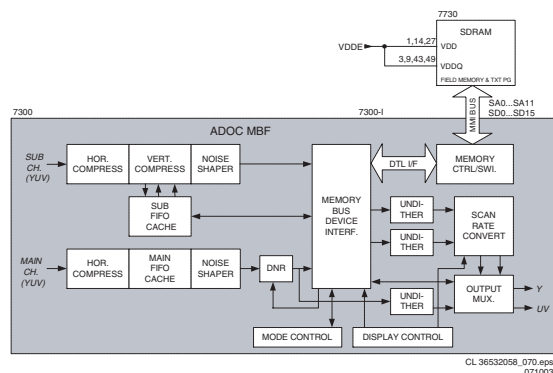


Figure 9-14 MBF block diagram

#### Back End Features (BEF)

The Back End Features (BEF) block embodies a collection of spatial picture enhancement functions.

The video display has to be blanked during AV switching, channel switching, V-chip, and Child Lock modes. This is done inside the BEF block of the ADOC IC. The fast blanking signal input from SCART1 and SCART3 (TV SCART inputs) for RGB video insertion is connected to the ADOC IC.

Sharpness functions are:

- Luminance Transient Improvement (LTI),
- Dynamic Peaking, and
- Digital Color Transient Improvement (DCTI).

The panorama block does the non-linear scaling for displaying 4:3 formats on a wide-screen display.

Color enhancement functions are:

- Skin Tone Control,
- Blue Stretch, and
- Green Enhancement.

A color Space Converter can convert the video signal from YUV to RGB format. The Frame Processing block can insert frames and borders such as a colored frame around the Picture in Picture (PIP). Following figure shows the structure of the Back End Feature block.

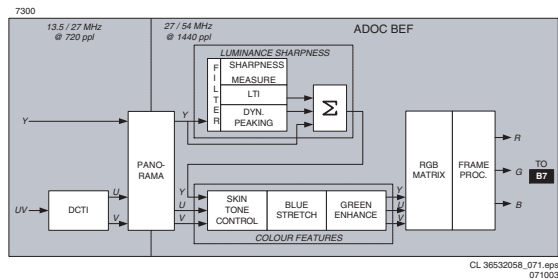


Figure 9-15 BEF block diagram

#### Digital Output Processor (DOP)

The DOP is a display processor block, and contains the following functions:

- **RGB control processor** with linear RGB input for the main video signal, a linear RGB input for OSD/text signals with blending, and an RGB output stage with black current stabilization which is realized with the continuous cathode calibration (2-point black current measurement) system.
- **Programmable deflection processor**, driven by an external crystal clock, which generates the drive signals for the horizontal, east-west, north-south and vertical deflection with extensive geometry correction capabilities.
- The circuit can be used in both single scan (50 or 60 Hz) and double scan (100 or 120 Hz) applications.

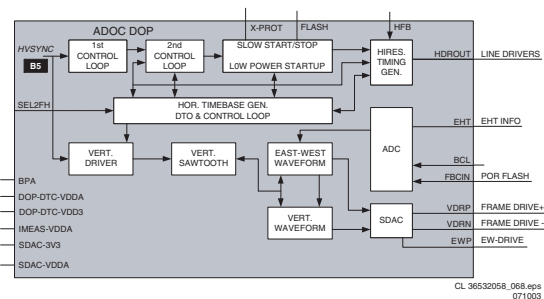


Figure 9-16 DOP block diagram



**RGB Control Processing**

- The RGB control circuit of the DOP contains two sets of input signals:
  - The first RGB input (RGB), 10 bits wide, is intended for the normal video signals coming from the BEF part. The "RGB" signals will first enter a contrast control stage, followed by a brightness control stage, both influenced by a combination of user control, Beam Current Limiter and Peak White Limiter, followed by a soft clipper stage. Then the signal will be applied to the blender stage. The blender input signal will be used as an input for the peak white limiting system.
  - The second RGB input (GFX), 4 bits wide, is intended for OSD and Teletext signals. The switching between the internal signal and the OSD signal is realized via a blending function. The "GFX" input signals will be re-formatted to 10 bits wide internally before entering the Beam Current Control brightness correction stage, followed by the hard clip stage. Then the signal will also be applied to the blender stage.
- The blender combines the two input data streams into one stream. A third data stream controls this blender.
- The next block is the "Drive Adjust" part. It contains a Picture Tube Biasing system, a Beam Current Control, and Peak White Limiting part.

In order to enhance the spatial bandwidth of the CRT display, Scan Velocity Modulation (SCAVER) is implemented on the CRT-panel.

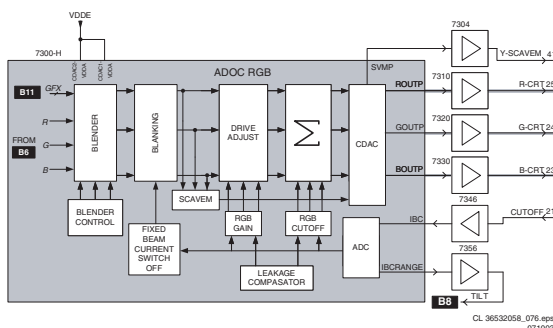


Figure 9-17 ADOC RGB control block diagram

**Synchronization and Deflection Processing**

- Horizontal synchronization and drive circuit.** The horizontal drive signal is obtained from an internal oscillator, which runs at a fixed frequency of 54 MHz. This oscillator is synchronized to the incoming horizontal H\_D pulse by means of a digital PLL. The horizontal drive signal is generated by a second control loop, which compares the phase of the reference signal (applied from the internal DTO) to the horizontal flyback pulse HFB.
- Vertical deflection and drive circuit.** The drive signals for the vertical and E/W deflection circuits are generated by a vertical divider, which derives its reference signal from the Horizontal Time base Generator. The incoming V\_D pulse, generated by the input processor or the Feature Box, synchronizes this divider. The vertical drive output is realized by a differential voltage, which is generated by SDACs. The outputs must be DC-coupled to the vertical output stage (TDA8177, item 7620 on the LSP).

See also figure "DOP block diagram"

**9.6 Synchronization****9.6.1 Sync Flow**

The CVBS signal on the SCART1/AV1 connector (CVBS-SC1\_AV1-IN system signal path; designated as EXT1 CVBS) is used to provide synchronization for the EXT1 RGB input. Besides providing synchronization for RGB source, EXT1 CVBS is also required for SCART2/AV2 CVBS output.

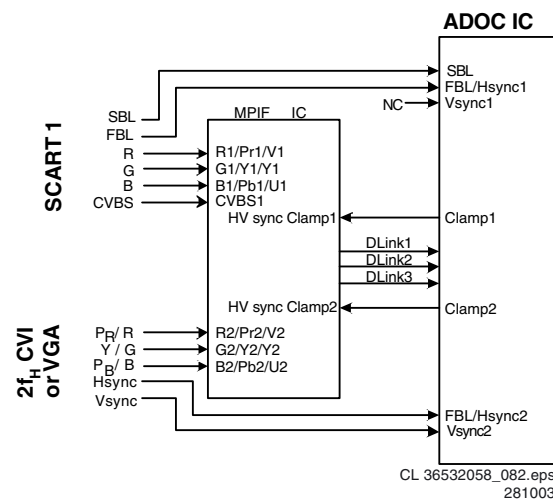


Figure 9-18 Sync flow block diagram

For 1fH CVI input, synchronization is derived from sync-on-Y. For the 2fH CVI input, synchronization signal is derived from sync-on-Y input or the H\_SYNC/V\_SYNC. In case of VGA input, synchronization signal is taken from H\_SYNC and V\_SYNC inputs. In case of HDMI input, synchronization signal is taken from H\_HDMI and V\_HDMI outputs of the HDMI panellink receiver.

**9.7 Audio****9.7.1 Introduction**

Sound IF processing, audio source selection, and audio analog-digital signal conversions are done in the MPIF IC. SIF demodulation, sound system auto-detection, audio base-band, and headphone processing is done in the ADOC IC. Therefore, the ADOC contains a digital TV sound processor for analog and digital multi-channel sound systems in TV sets. By hardware programming, several applications can be scaled.

The sound processing of the SALSA system can be split into three parts:

- Initial source selection and analog to digital conversion performed by MPIF.
- Demodulator and Decoder (DEMDEC) performed by the ADOC.
- Back End Features (BEF) performed by the ADOC.

**9.7.2 MPIF Sound part**

The (main) Tuner receives an RF signal and converts it to IF. Via the appropriate SAW filters, the SIF signal is delivered to the QSS mixer stage of the MPIF IC and if channels according to standard L/L' are received also to the AM demodulator. The Quasi Split Sound demodulation generates the SSIF or intercarrier signal. By the SSIF switch, it is possible to choose between the internally derived intercarrier and an external second SIF (e.g. from a PIP front end or 10.7 MHz radio). The

selected SSIF passes some anti-alias filtering, is amplified in an AGC amplifier and is then converted from analog to digital (SSIF AGC/ADC). Together with other signals, the digitized SSIF is transferred via an I2D-Link to the ADOC IC. The audio signal out of the AM demodulator is connected to the analog X-bar in the MPIF IC. All other inputs to this multiplexer/ audio switch come from external, either from the PIP front end (AMEXT/PIPMONO) or SCART/CINCH (AUDxin) or the DAC1, DAC2 output signals from ADOC. The audio AD converters are digitizing the audio signals foreseen for further digital processing in ADOC. Three stereo outputs (AUDx out, LINE out) are available for connections to SCART/CINCH sockets. The sound part of ADOC consists of the demodulator/decoder (DEMDEC), sample rate conversion (SRC), a digital input X-bar, the digital audio processing for the loudspeaker, headphone and DAC channels, the I2S processing and interfacing as well as the DA conversion. This part will be described in the next chapter.

### 9.7.3 ADOC Sound part

#### Introduction

The ADOC sound part contains two DSP cores as shown in the block diagram. The first core called DEMDEC-DSP is combined with DEMDEC (Demodulation/Decoding) hardware and the second core is the AUDIO-DSP. The DEMDEC-DSP is used for the decoder and demodulator tasks, plus the sample rate conversion.

The AUDIO-DSP is used for the sound features, from the level adjust unit up to the output cross bar. Audio DACs and I2S hardware (optional) are converting the processed signals to analog or digital audio.

All I2D data links carry sound signals. The data link processing splits them from the other signals as video so that the DEMDEC block receives the second sound IF (SSIF) and the audio signals from the audio ADCs of the MPIF IC. The SSIF needs some hardware processing before it enters the DEMDEC DSP. The DEMDEC processing will be described in the next chapter. The audio signals from the audio ADCs of the MPIF are passing the DEMDEC DSP only for source selection and sample rate conversion.

In this chassis, two of the DAC **outputs** are used to feed a headphone. Two other DAC stereo outputs are provided for the audio feedback to the MPIF IC. They are located to pins of the ADOC that suit best for connection to MPIF.

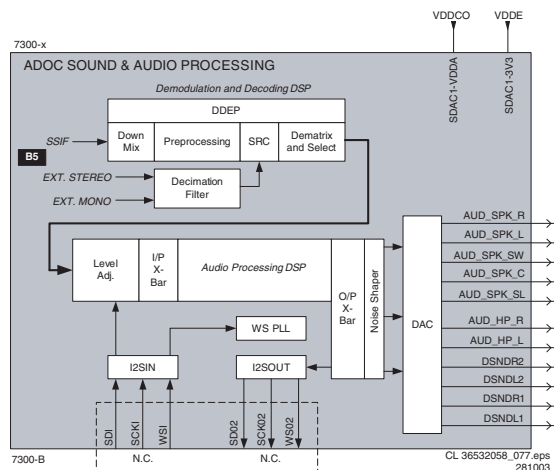


Figure 9-19 ADOC sound processing block diagram

#### DEMDEC DSP

The output signals of the above-mentioned hardware blocks, plus four audio ADC channels are read in by the DEMDEC DSP, processed, converted to the current audio sample rate,

"demultiplexed", and forwarded to the Audio DSP for further processing (volume, tone control, effects etc.).

#### Down Mixer

The digitized SSIF input signal is fed to the mixers, which mix one or both input sound carriers down to zero IF.

#### Pre-processing

This part contains the sound system identification and demodulation circuitry.

#### Audio Sample Rate Conversion (SRC)

All input signals pass through a sample rate conversion to the actual output sample rate (usually 48 kHz) such that the output rate does not need to be synchronized with any of the input rates. Up to five separate channels can be converted.

#### Audio Processing DSP

This block applies several filters, like down-sampling and de-emphasis, noise reduction processing, performs a sample rate conversion (SRC) to the current audio sample rate, and routes the decoded signals to the output channels.

The generic processing controls are Volume, Bass, Treble, Balance, Incredible Surround, Spatial (incredible mono), DBE, Dynamic Ultra Bass II (for non-woofer sets only), AVL, Sub-Woofer, and 5-band Graphic equalizer.

The Headphone volume can be separately controlled in the Headphone menu without affecting the master volume (the setting of the volume tables will be adapted after fine tuning). For variable volume output for USA, the DAC1 output will switch to the Main channel and therefore the same volume curve for the Main Channel can be used.

### 9.7.4 Audio Amplifier

#### Speakers (diagram A6)

The audio output stage is built around IC7701, which is a balanced amplifier, and is located on the LSP. It uses a monolithic integrated power amplifier IC, the TDA7497. The gain of the amplifier is constant. This means that volume control is done via the ADOC.

The supply voltage is +28 V, generated by the power supply via L5506 (or L5512). The TDA7497 delivers an output of 3 x 10 W<sub>rms</sub> to two full range speakers and a (optional) subwoofer.

#### Muting

There are three types of muting available: system mute, headphone status mute, and user mute.

- **System mute.** System muting is implemented for "special events" such as channel/source change event, loss of identification signal, "on/off" switching of the set, during search and auto store/program, and/or sound mode change. This muting is transparent to the user. Audio output is muted before the above "special events" occurred, to prevent problems such as audible plop. Muting is done via the SOUND-ENABLE (software controlled) and/or POR (hardware controlled) line connected (via TS7710 and 7711) to pin 10 of the amplifier-IC and coming from the ADOC microprocessor.
- **Headphone status mute.** A headphone status is available to detect the presence of the headphone and mute the main speakers if the headphone is detected. The microprocessor will read the FRONT-DETECT status.
- **User mute.** This is a mute option available to the user. The user select the MUTE option on the remote control to switch "off/on" the sound output to the main loudspeaker and the (optional) subwoofer.

#### Headphone amplifier (diagram A7)

The headphone amplifier is built around IC7751 (NJM4556), which is a high-gain, high output current dual operational amplifier. The supply voltage is +5 V.



## 9.11 Abbreviation list

Table 9-1 Abbreviations

Abbreviation	Description
0/6/12	SCART switch control signal on A/V board. 0 = loop through (AUX to TV), 6 = play 16:9 format, 12 = play 4:3 format
2CS	2 Carrier Stereo
A2	Commonly known as two carriers sound (2CS) system
AC (or ac)	Alternating Current
ACI	Automatic Channel Installation: algorithm that installs TV channels directly from a cable network by means of a predefined TXT page
ADC	Analogue to Digital Converter
ADOC	Analogue Digital One Chip
AFC	Automatic Frequency Control: control signal used to tune to the correct frequency
AGC	Automatic gain control (feedback) signal to the tuner.
AM	Amplitude Modulation
ANR	Automatic Noise Reduction: one of the algorithms of Auto TV
AP / A/P	Asia Pacific
AR	Aspect Ratio: 4 by 3 or 16 by 9
ASD	Automatic Standard Detection
AV	External Audio Video
AVL	Automatic Volume Level control
B	Blue
B/G	Monochrome TV system. Sound carrier distance is 5.5 MHz
BBD	Black Bar Detection
BCL	Beam Current Limiter
BC-PROT	PROtection signal to the microprocessor for a too high Beam Current.
BG	System B and G
BLC-INFO	BLack Current INFO
BLD	Black Level Detection
BS	Black Stretch
BTSC	Broadcast Television Standard Committee. Multiplex FM stereo sound system, originating from the USA and used e.g. in LATAM and AP-NTSC countries
C	Chroma (video) / Centre channel (audio)
CL	Constant Level: audio output to connect with an external amplifier
CLUT	Colour Look Up Table
ComPair	Computer aided rePair
CRT	Cathode Ray Tube or picture tube
CSM	Customer Service Mode
CTI	Colour Transient Improvement: manipulates steepness of chroma transients
CVBS	Composite Video Blanking and Synchronization
CVI	Component Video Input
DK	Monochrome TV system. Sound carrier distance is 6.5 MHz
DAC	Digital to Analogue Converter
DBE	Dynamic Bass Enhancement: extra low frequency amplification
DC (or dc)	Direct Current
DCC	Dynamic Contrast Control
DC-filament	Filament supply voltage
DEGAUSS	Control line. Logic LOW to enable CRT degaussing. Logic HIGH to disable the CRT degaussing.
DFU	Directions For Use: owner's manual
DNR	Digital Noise Reduction: noise reduction feature of the set
DOP	Digital Output Processor (Part of ADOC which takes care of RGB control and delection)
DPL	Dolby Pro Logic
DRAM	Dynamic RAM
DS	Digital Scan
DSP	Digital Signal Processing
DST	Dealer Service Tool: special remote control designed for dealers to enter e.g. service mode (a DST-emulator is available in ComPair)
DTS	Digital Theatre Sound
DVD	Digital Versatile Disc
DVI(-d)	Digital Visual Interface (d= digital only)
DW	Double Window
DYN-FASE-COR	Dynamic phase correction, to correct the phase of the H-drive
EEPROM	Electrically Erasable and Programmable Read Only Memory
EHT	Extra High Tension
EHT-INFO	Extra High Tension INFOrmation, used for contrast reduction, vertical and horizontal amplitude correction, beam current protection, and flash detection

Abbreviation	Description
EMI	Electro Magnetic Interference
EPG	Electronic Program Guide: system used by broadcasters to transmit TV guide information (= NextView)
EPLD	Erasable Programmable Logic Device
EU	Europe
EW	East West, related to horizontal deflection of the set
EW-DRIVE	East -West correction drive signal.
EXT	EXTernal (source), entering the set by SCART or by Cinches (jacks)
FBL	Fast BLanking: DC signal accompanying RGB signals
FBX	Feature Box: module which contains 100 Hz processing, Pixel Plus, and AutoTV algorithms (FBX6= based on PICNIC, FBX7= based on PICNIC and Eagle)
FE	Front End
Field	Each interlaced broadcast FRAME is composed of two Fields, each Field consists of either Odd or Even lines
FILAMENT	Filament of CRT
FLASH	FLASH memory
FM	Field Memory / Frequency Modulation
FM Radio	Audio receiver which can receive the FM Band 87.5 - 108 MHz
FMR	FM Radio
Frame	A complete TV picture comprising of all lines (625/525)
FRAMEDRIVE -	Differential frame (vertical) drive signal (negative)
FRAMEDRIVE +	Differential frame (vertical) drive signal (positive)
FRC	Frame Rate Converter
FRONT-DETECT	Control line for detection of headphone insertion, Service Mode jumper, power failure detection.
FRONT-Y_CVBS	Front input luminance or CVBS (SVHS)
G	Green
Gb/s	Giga bits per second
H	H_sync to the module
H_2FH	Horizontal sync input for the 2FH source.
H_A50	Horizontal Acquisition 1fH: horizontal sync pulse coming out of the HIP
H_D100	Horizontal Drive 2fH: horizontal sync pulse coming out of the feature-box
H_DRIVE	Horizontal Drive
H_FLYBACK	Horizontal Flyback
H_OUT	H_sync output of the module
H_OUT	Horizontal Output pulse
HA	Horizontal Acquisition: horizontal sync pulse coming out of the BOCMA
HD	High Definition
HDMI	High Definition Multimedia Interface: Interface that supports RGB or YCbCr digital video at rates up to 5Gbps, up to eight channels of digital audio, along with a AV-link capability. Is meant as successor of DVI.
HEADPHONE -L	Stereo headphone (Left) signal output.
HEADPHONE -R	Stereo headphone (Right) signal output.
HFB	Horizontal Flyback Pulse: horizontal sync pulse from large signal deflection
HP	HeadPhone
HW	Hardware
I	Monochrome TV system. Sound carrier distance is 6.0 MHz
I2C	Integrated IC bus (same as IIC)
I2S	Integrated IC Sound bus
IC	Integrated Circuit
IDRIVE-	Vertical drive -
IDRIVE+	Vertical drive +
IF	Intermediate Frequency
IF-TER	IF signal from main tuner
IIC	Integrated IC bus (same as I2C)
Interlaced	Scan mode where two fields are used to form one frame. Each field contains half the number of the total amount of lines. The fields are written in "pairs", causing line flicker.
IO	In/Out
IR	Infra Red
IROM	Internal ROM (inside uP)
IRQ	Interrupt ReQuest
ITV	Institutional TV
JTAG	Joint Test Action Group. Definition for a standardised serial test interface
KEYB	Front panel keyboard

Abbreviation	Description
KEYBOARD	Input line: carries the voltage value of the corresponding tact switch on TOP-control or FRONT-control keypad
L	Left audio channel
L/L'	Monochrome TV system. Sound carrier distance is 6.5 MHz. L' is Band I, L is all bands except for Band I
Last Status	The settings last chosen by the customer and read and stored in RAM or in the NVM. They are called at startup of the set to configure it according to the customer's preferences
LATAM	Latin America
LCD	Liquid Crystal Display
L-CL_VLOUT	REAR CINCH stereo output
LED	Light Emitting Diode
LFE	Low Frequency Enhancement audio channel
L-FRONT-IN	EXT3 stereo input
LIGHT-SENSOR	Ambient light intensity signal.
LINE DRIVE	Line drive signal (for the Line transistor)
LINEDRIVE1	Horizontal (line) deflection drive signal.
LNA	Low Noise Adapter / Low Noise Amplifier
LOT	Line Output Transformer
LPD	LG.Philips Displays
LS	Loudspeaker
Ls, Rs	Left surround and Right surround channel (audio)
LSP	Large signal panel
Lt, Rt	Left total and Right total in case of a Dolby ProLogic encoded signal (audio)
LTI	Luminance Transient Improvement
LTP	Luminance Transient Processor
LUT	Look Up Table
LVDS	Low Voltage Differential Signalling, data transmission system for high speed and low EMI communication.
M/N	Monochrome TV system. Sound carrier distance is 4.5 MHz
Mb/s	Mega bits per second
MCS	Multi Channel Sound: refers to Dolby Pro Logic Surround in A02 ADOC
MDO	Mode control data output
MIPS	Microprocessor without Interlocked Pipeline-Stages. A RISC-based microprocessor.
Mips	Million instructions per second
MMI	Multi Media Interface
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MPEG	Motion Pictures Experts Group
MPIF	Multi Platform InterFace (Part of Salsa chipset, sister-chip of ADOC IC)
MPIP	Multi Picture in Picture: commercial feature showing several frozen or moving pips
MPX	MultiPleX
MSP	Multi-standard Sound Processor: ITT sound decoder
MUTE	MUTE Line
NAFTA	North American Free Trade Area (NAFTA & USA are used interchangeably)
NC	Not Connected
NDF	No vertical Deflection: vertical fly back protection
NHF	No Horizontal deflection: horizontal fly back protection
NICAM	Near Instantaneously Companded Audio Multiplexing. This is a digital sound system, mainly used in Europe.
NTC	Negative Temperature Coefficient, non-linear resistor
NTSC	National Television Standard Committee. Colour system mainly used in North America and Japan. Colour carrier NTSC M/N= 3.579545 MHz, NTSC 4.43= 4.433619 MHz (this is a VCR norm, it is not transmitted off-air)
NVM	Non Volatile Memory: IC containing data such as alignments, stations
O/C	Open Circuit
OB	Option Byte
OC	Open Circuit
ON/OFF LED	On/Off control signal for the LED
ON/STBY	On/Standby
ON-OFF-LED	Active-LOW control line. Logic LOW = red LED on, HIGH = red LED off.
OP	Option Byte
OSD	On Screen Display
P50	Project 50: communication protocol between TV and peripherals
PAL	Phase Alternating Line. Colour system mainly used in West Europe (colour carrier= 4.433619 MHz) and South America (colour carrier PAL M= 3.575612 MHz and PAL N= 3.582056 MHz)
PC	Personal Computer

Abbreviation	Description
PCB	Printed Circuit Board (same as "PWB")
PCM	Pulse Code Modulation
PILOT	Pilot Signal
PIP	Picture In Picture
PLL	Phase Locked Loop. Used for e.g. FST tuning systems. The customer can give directly the desired frequency
POR	Power On Reset, signal to reset the microprocessor
POR_FLASH	Signal that informs the micro controller (painter) that set will switch off
Progressive Scan	Scan mode where all scan lines are displayed in one frame at the same time, creating a double vertical resolution.
PTC	Positive Temperature Coefficient, non linear resistor
PTP	Picture Tube Panel
PWB	Printed Wiring Board (same as "PCB")
PWM	Pulse Width Modulation
QSS	Quasi Split Sound
R	Right audio channel
R	Red
RAM	Random Access Memory
RC	Remote Control transmitter
RC5	Remote Control system 5, the signal from the remote control
RC5 / RC6	Signal protocol from the remote control receiver
RDS	Radio Data System
RESET	RESET signal
RF	Real Flat / Radio Frequency
RGB	Red, Green, and Blue. The primary colour signals for TV. By mixing levels of R,G, and B, all colours (Y/C) are reproduced.
RGBHV	Red, Green, Blue, Horizontal sync, and Vertical sync
RISC	Reduced Instructions Set Computer
RMS	Root Mean Square value
ROM	Read Only Memory
S	Surround channel or mono surround channel (audio)
S/C	Short Circuit
S/PDIF	Sony Philips Digital InterFace
SALSA	System Application for Low Segment of Analogue TV
SAM	Service Alignment Mode
SAP	Second Audio Program
SAW	Surface Acoustics Wave
SC	SandCastle: two-level pulse derived from sync signals / SCART
SCART	Syndicat des Constructeurs d'Appareils Radiorecepteurs et Televisieurs
SCAVEM	Scan Velocity Modulation
SCL	Serial Clock I2C
SCL-F	Clock Signal on Fast I2C bus
SD	Standard Definition
SDA	Serial Data I2C
SDA-F	Data Signal on Fast I2C bus
SDAM	Service Default / Alignment Mode
SDRAM	Synchronous DRAM
SECAM	SEquence Couleur Avec Memoire: Colour system mainly used in France and East Europe. Colour carriers= 4.406250 MHz and 4.250000 MHz
SEL	Control signal
SIF	Sound Intermediate Frequency
SIMM	Single In-line Memory Module: 80-fold connector between LSP and SSB
SL	Audio Surround Left
SLDP	Smart Local Dooming Prevention (HW and SW)
SMC	Surface Mounted Components
SMPS	Switched Mode Power Supply
SND	SouND
SNERT	Synchronous No parity Eight bit Reception and Transmit
SOG	Sync On Green
SOPS	Self Oscillating Power Supply
SOUND-ENABLE	Control line to do hardware mute or un-mute of loudspeakers.
SR	Audio Surround Right
SRAM	Static RAM
SS	Small Screen
ST_BY	Standby
STANDBY (POR)	Signal coming from Main Supply informing the supply is switching off
STATUS	Status signal from pin 8 on SCART connector
STBY	Standby
SURR	Surround (mono) signal
SVHS	Super Video Home System



Abbreviation	Description
SW	Software / Subwoofer
SW1	Switch 1
TBD	To Be Defined
THD	Total Harmonic Distortion
TILT	PWM Output signal (variable DC level) to control the picture tilt from the DOP block of the ADOC.
Trinorma	Video standard, combination of PAL N, PAL M, NTSC M
TXT	Teletext
TXTSW	Teletext switch
U_100	U from Feature Box
UART	Universal Asynchronous Receiver Transmitter
UBE	Ultra Bass Enhancement
uC	Micro controller
UI	User Interface
UOC	Ultimate One Chip
uP	Microprocessor
UV	Colour difference signals
V	V_sync
V_100	V from Feature Box
V_2FH	Vertical sync input for the 2fH source.
V_A50	Vertical Acquisition 1fH
V_AMP	Vertical Amplitude DAC output
V_BAT	Main supply for deflection (usually 141 V)
V_D100	Vertical Drive 2fH: vertical sync pulse from deflection
V_DNEG	One of the symmetrical drive signals for the DC frame output stage.
V_DPOS	One of the symmetrical drive signals for the DC frame output stage.
V_OSD	Vertical OSD
VA	Vertical Acquisition
VBI	Vertical Blank Interval
V-chip	Violence chip
VCR	Video Cassette Recorder
VD	Vertical Drive: vertical sync pulse coming from the feature box
VDS	Virtual Dolby Surround
VERT	Vertical Output pulse
VESA	Video Electronics Standards Association
VGA	Video Graphics Array: 640x480 (4:3)
VGND	Video ground
VGUARD	Vertical guard voltage
VIF	Video Intermediate Frequency
VL	Variable Level out: processed audio output toward external amplifier
VMEM	Voltage supplied for EEPROM
VMICRO	Power supply for micro controller
VOL	Volume
VSNC	Pulse derived of 530 s-circuit behind the HOP, to vertically synchronize the Painter
WD	Watch Dog
WE-NVM	NVM write enable control line.
WS	Wide Screen
WSS	Wide Screen Signaling, used by broadcasters to transmit e.g. PALPLUS and Aspect Ratio
WST	World System Teletext
WXGA	1280x768 (15:9)
WYSIWYR	What You See Is What You Record: record selection that follows main picture and sound
XGA	Extended Graphics Array: 1024x768 (4:3)
XTAL	Quartz crystal
Y	Luminance signal
YC (or Y/C)	Luminance (Y) and Chrominance (C) signal (analogue video encoding format)
YPbPr	Component video (Y= Luminance, Pb/ Pr= Colour difference signals)
YUV	Component video

## 9.12 IC Data Sheets

This section shows the internal block diagrams and pin layouts of ICs that are drawn as "black boxes" in the electrical diagrams (with the exception of "memory" and "logic" ICs).

### 9.12.1 Diagram M1, Sil 9993 (IC7002)

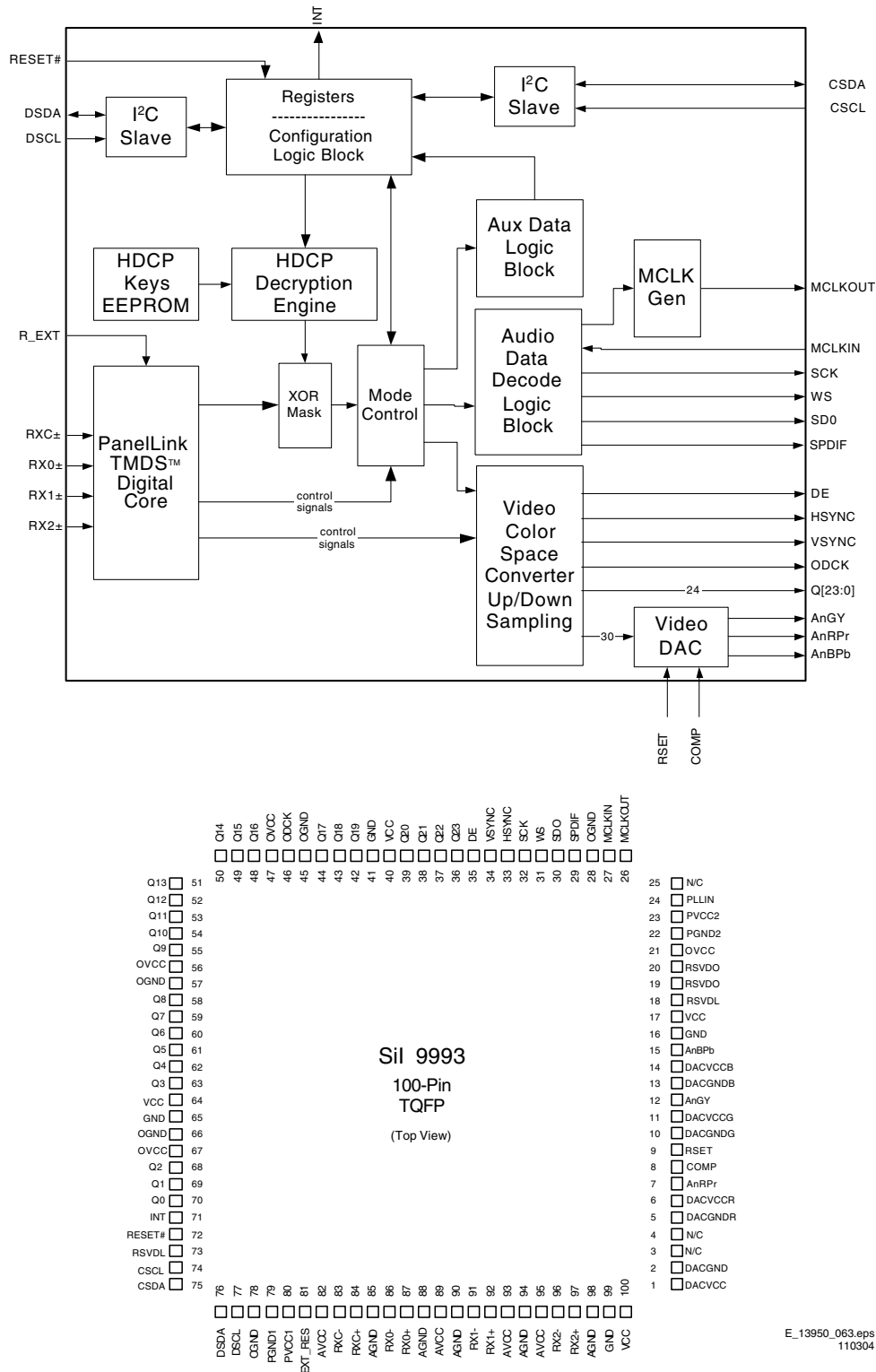
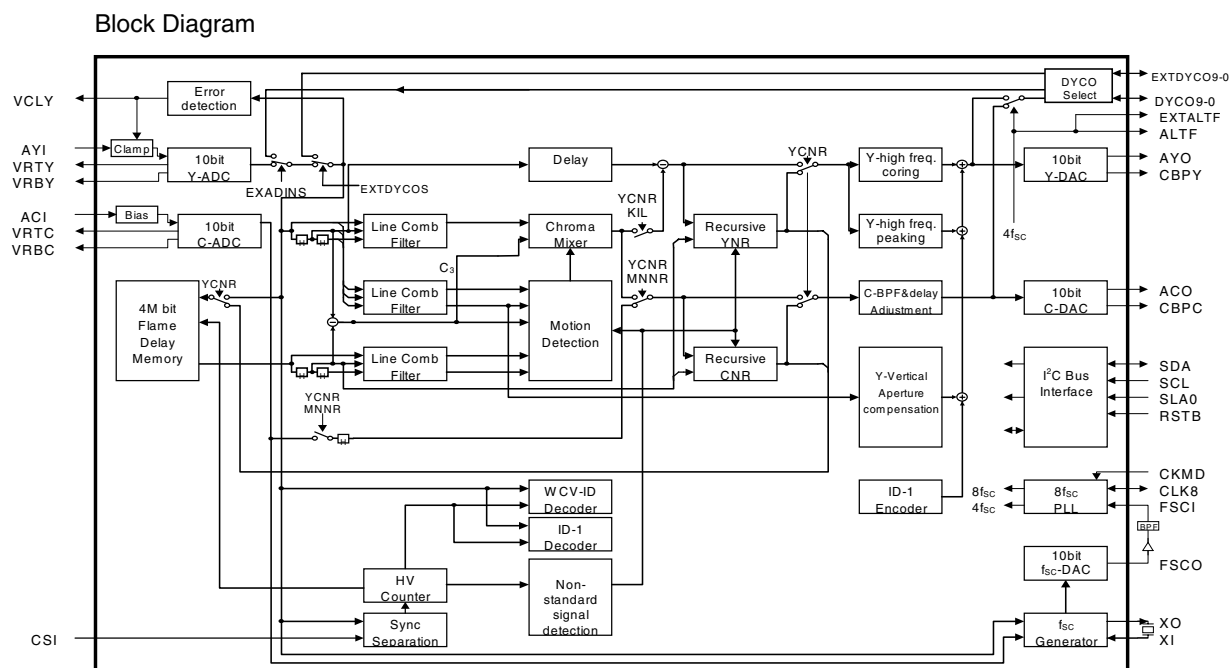


Figure 9-21 Internal block diagram and pin configuration

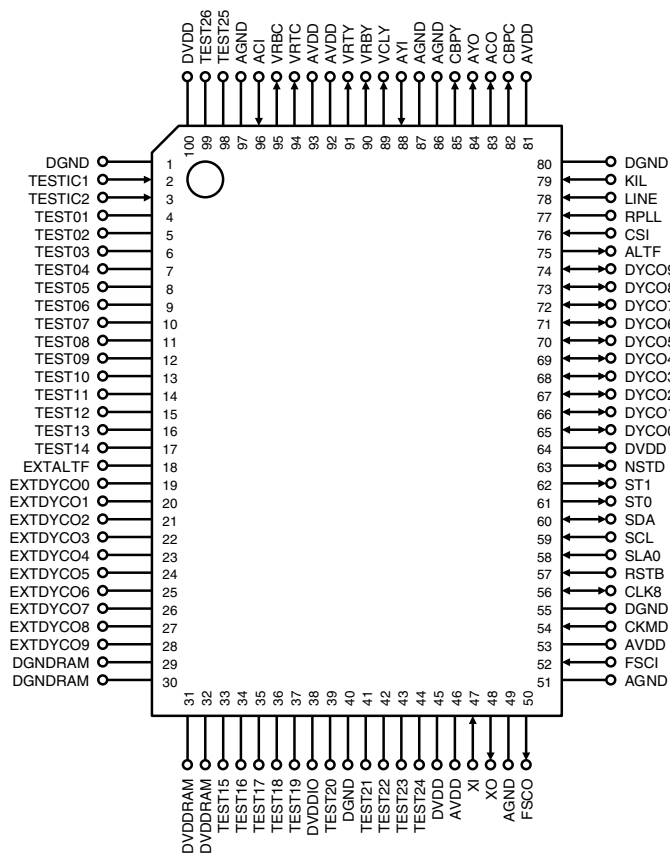
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## 9.12.2 Diagram B17, uPD64083 (IC7823)



## Pin Configuration (Top View)

100-pin plastic QFP (14 20)  
PD64083GF-3BA



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Figure 9-22 Internal block diagram and pin configuration



# 10. Spare Parts List

Not applicable.

## 11. Revision List

First release.